INSTRUCTION MANUAL

DATA ACQUISITION SYSTEM TIME STANDARD

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SECTION 1
GENERAL DESCRIPTION

1.1 GENERAL INFORMATION

A. Scope of Manual

This manual contains information concerning the description and operation of the time standard which forms an integral part of the Gilmore Creek Data Acquisition Site ground instrumentation equipment.

B. Acquisition System Concept

The data acquisition system has two basic functions: (1) to provide information concerning the position of a vehicle in space, and (2) to provide means of acquiring and demodulating telemetry information transmitted from the vehicle.

The data acquisition site contains the equipment required to perform these functions and to allow monitoring of station operation during tracking operations. The site is to be used in meteorological and communication satellite programs.

C. Time System Functions

The timing system provides accurate time-of-day information so that tracking and telemetry data may be correctly oriented with respect to time. Synchronizing pulses are also supplied to data-processing equipment. In addition, time-of-day displays and other equipment receive signals generated by the timing equipment. The timing signals developed are usually recorded or used simultaneously with various other data of the data acquisition operation. This time validates the information for immediate processing or future use. Because of the geographical location of the data acquisition sites, complete coverage of each satellite is possible.

The timing system is synchronized to Radio Station WWV to within 1 or 2 milliseconds, with the uncertainties and variations in the propagation delay time of the WWV timing signal being the major cause of error in time synchronization.

D. Abbreviations Used

BCD	Binary Coded Decimal
Bit	Binary Digit
BTC	Binary Time Code
DOY	Day of Year
GMT	Greenwich Mean Time
LSB	Least Significant Bit
MSB	Most Significant Bit
PPS	Pulse(s) Per Second
PPM	Pulse(s) Per Minute
PWC	Pulse Width Coded
PDM	Pulse Duration Modulation
PWM	Pulse Width Modulation
SDTC	Serial Decimal Time Code
TCW	Time Code Word
TOD	Time of Day
TOY	Time of Year

E. Equipment Supplied

Table 1.1 lists the commercial equipment used in the timing system.

TABLE 1.1. EQUIPMENT SUPPLIED

EQUIPMENT	MANUFACTURER	INSTRUCTION MANUAL
HP 104 AR Quartz Oscillator	Hewlett-Packard Company	Operating and Service Manual 104 Quartz Oscillator
Model 905 WWV Receiver	Beckman/Berkeley Division	Instruction Manual WWV Receiver Model 905
Type 503 Cathode-Ray Oscilloscope	Tektronic	Instruction Manual Type 503 Cathode-Ray Oscilloscope
RP-32 Power Supply and S-pac Digital Modules	Computer Control Company, Inc.	Instruction Manual S-pac Digital Modules

1.2 DESCRIPTION OF THE TIMING SYSTEM

A. General

The timing system consists of a time standard rack which houses all of the time generating equipment and all connections to other equipment which use the output signals from the rack.

The following paragraphs present both a physical and functional description of the time standard rack and of all the units mounted in it.

B. Physical Description

The time standard, Figures 1.1, 1.2, 1.3, and 1.4, consists of two equipment cabinets bolted together to form a double equipment rack. This rack houses all of the time signal generating equipment and all connections to other equipment which use the output signals from the time standard.

Cooling of the equipment is provided by two blowers mounted on top of the cabinet. Interrack cabling provides power to the various units. Signal outputs are cabled to connectors at the top of the right-hand cabinet. Access to the cabling and to the rear of each unit is obtained by opening the double-hinged doors at the rear of the cabinet.

Double front doors, with glass enclosed cutouts, allow the operating controls and the meters to be monitored. Opening these doors provides access to the front of each unit. The following paragraphs describe the physical aspects of each unit:

1. Power Control Panel

The Power Control Panel, Figure 1.5, is located at the top of the right-hand cabinet. It occupies 5 1/4 inches of vertical rack space. Two operating controls are located on the front of this panel, the "AC Power" switch (15-amp circuit breaker) with lamp to indicate "ON" conditions and a "Voltage Monitor" switch with associated dc voltmeter which allows the dc voltages from the system power supply to be metered. Also mounted on this panel is the "Elapsed Timing" meter. This meter, which is controlled by the "AC Power" switch, displays the system operating time.

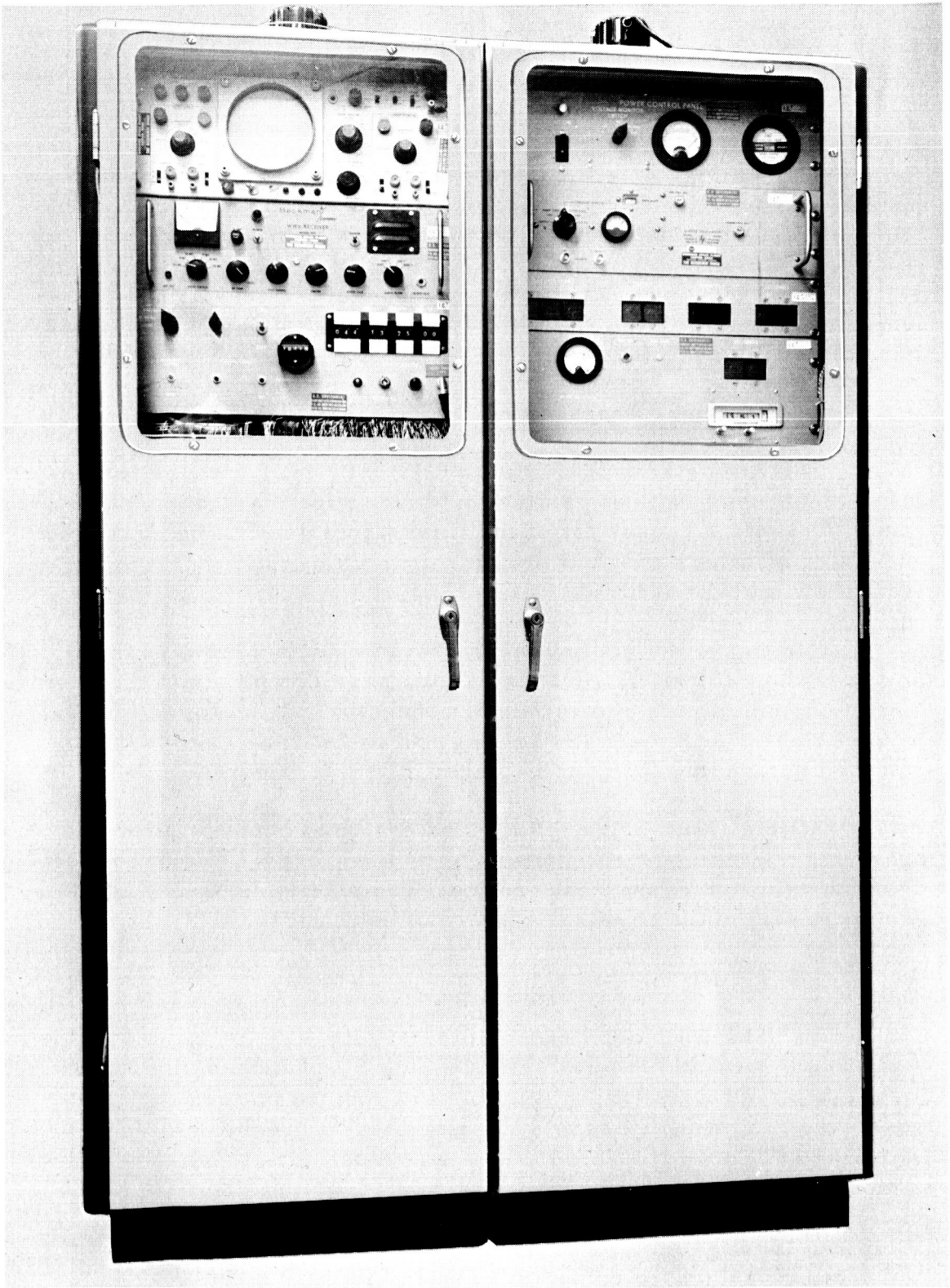


FIGURE 1.1 FRONT VIEW OF TIME STANDARD (DOORS CLOSED)

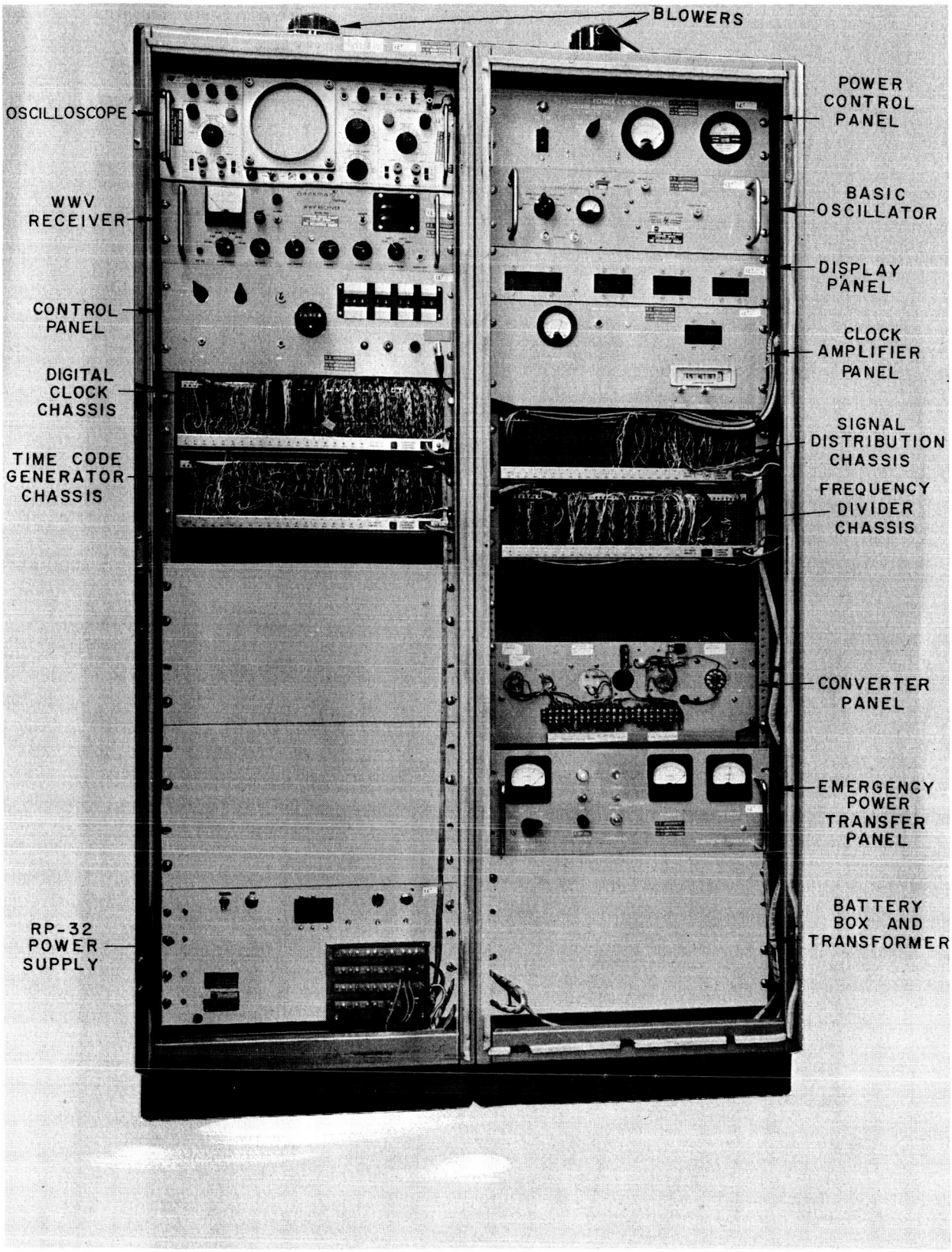


FIGURE 1.2 FRONT VIEW OF TIME STANDARD (DOORS OPEN)

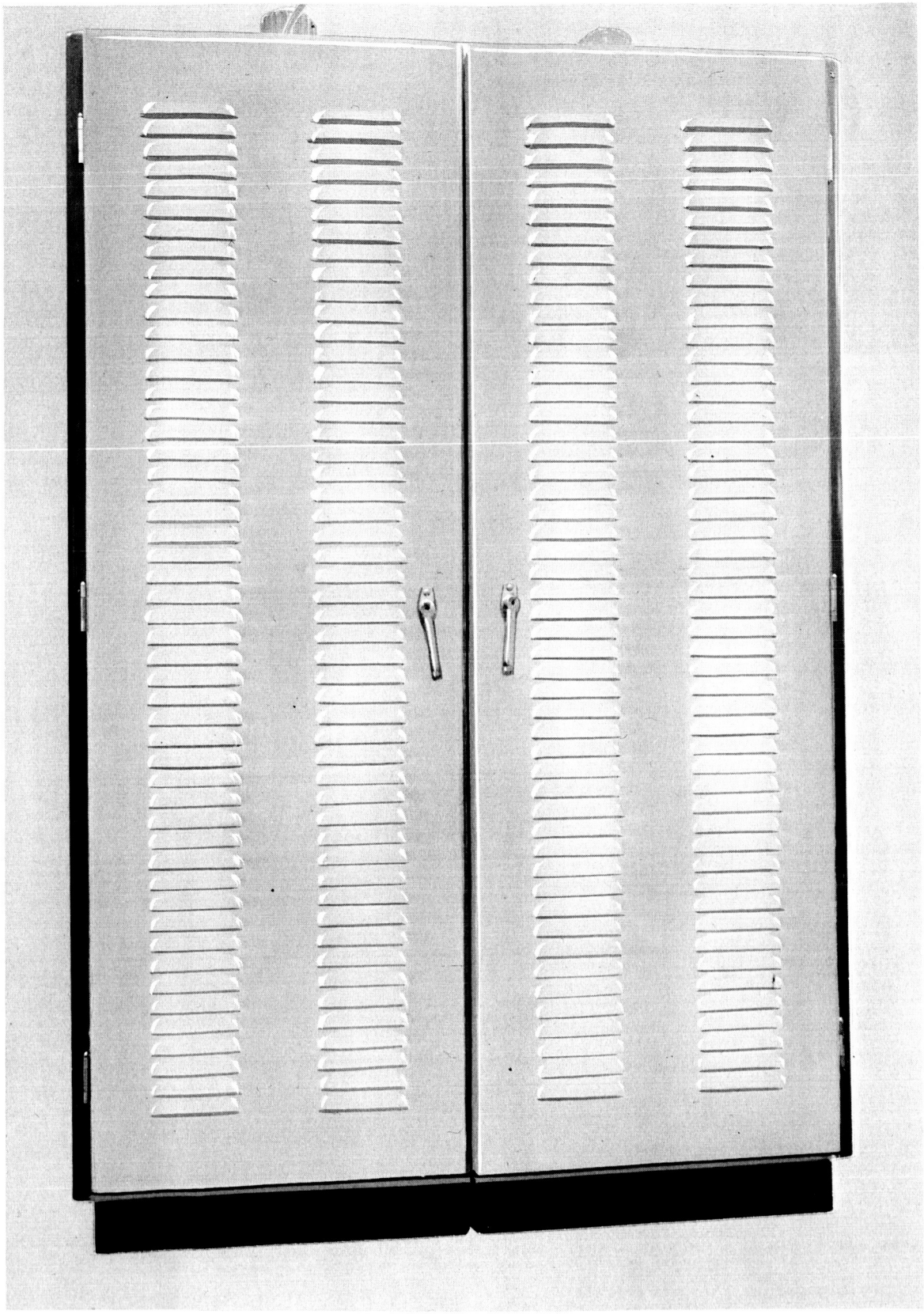


FIGURE 1.3 REAR VIEW OF TIME STANDARD (DOORS CLOSED)

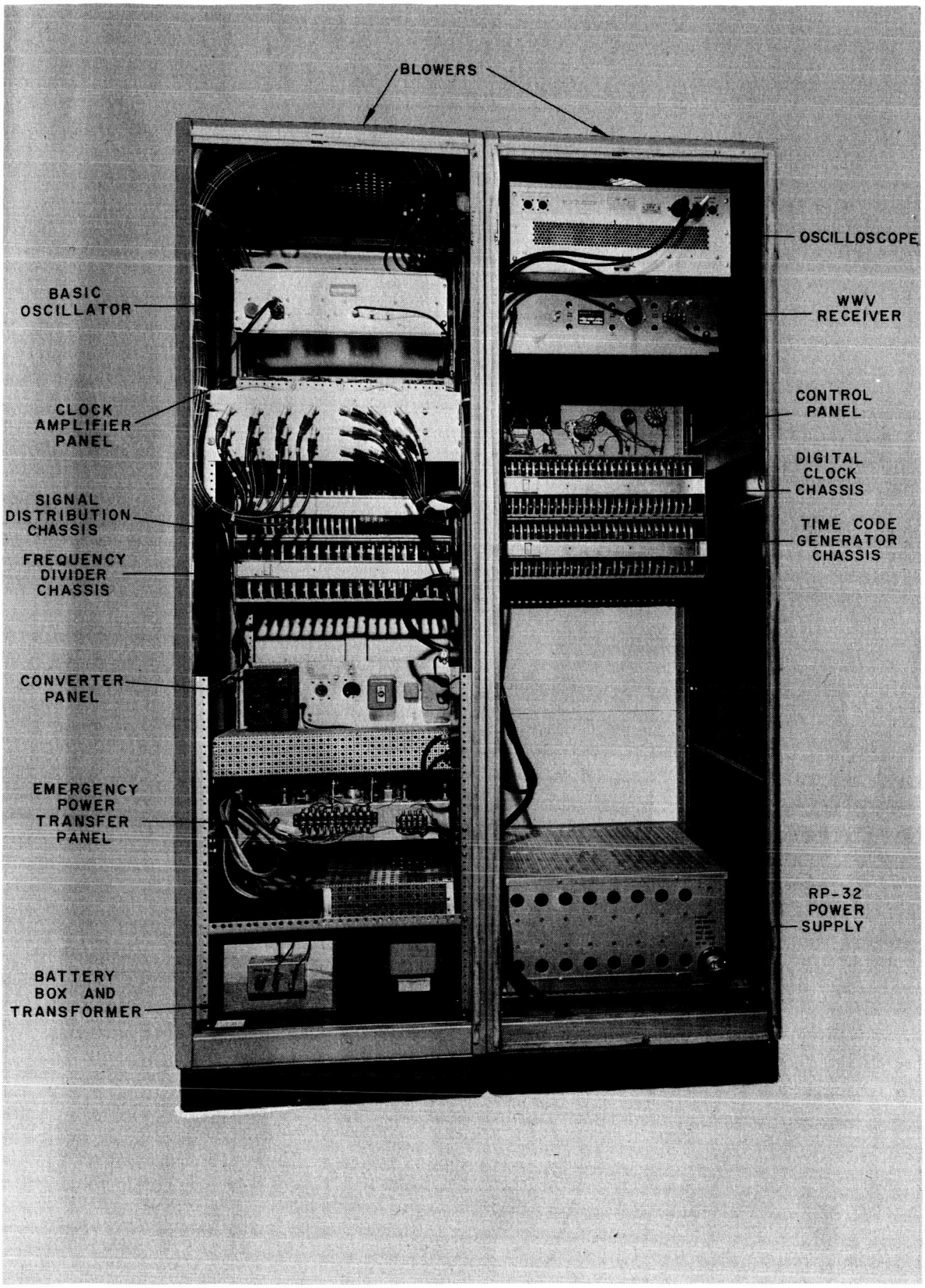


FIGURE 1.4 REAR VIEW OF TIME STANDARD (DOORS OPEN)

2. HP 104 AR Oscillator Panel

The HP 104 AR Oscillator Panel, Figure 1.6, is the second panel from the top of the right-hand cabinet. It occupies 5 1/4 inches of vertical rack space. A complete description of this unit can be found in the manufacturer's instruction manual referenced in Table 1.1.

3. Display Panel

The Display Panel, Figure 1.7, is the third panel from the top of the right-hand cabinet. It occupies 3 1/2 inches of vertical rack space. This panel contains nine digital decoders and indicating tubes which display Greenwich mean time in days of the year, hours, minutes, and seconds.

4. Clock-Amplifier Panel

The Clock-Amplifier Panel, Figure 1.8, is the fourth panel from the top of the right-hand cabinet. It occupies 7 inches of vertical rack space. Located on this panel is a meter which is used to monitor the output of the 60 cps amplifier.

This panel also contains two digital indicator tubes which display the seconds and tens of seconds output from the frequency divider, a numechron panel clock with provisions for setting the hours and minutes to a predetermined time, and a "Time Set" switch which is used to start and stop the numechron clock.

5. Signal Distribution Panel (Chassis)

The signal distribution unit, Figure 1.9, is the fifth panel from the top of the right-hand cabinet. It occupies 5 1/4 inches of vertical rack space. When mounted in the cabinet it is covered with a plain panel. The outputs from the timing system are connected from the rear of this panel to the output connectors at the top of the left-hand cabinet.

6. Frequency Divider Panel (Chassis)

The frequency divider unit is the sixth unit from the top of the right-hand cabinet. It occupies 5 1/4 inches of vertical rack space. When mounted in the cabinet it is covered with a plain panel.

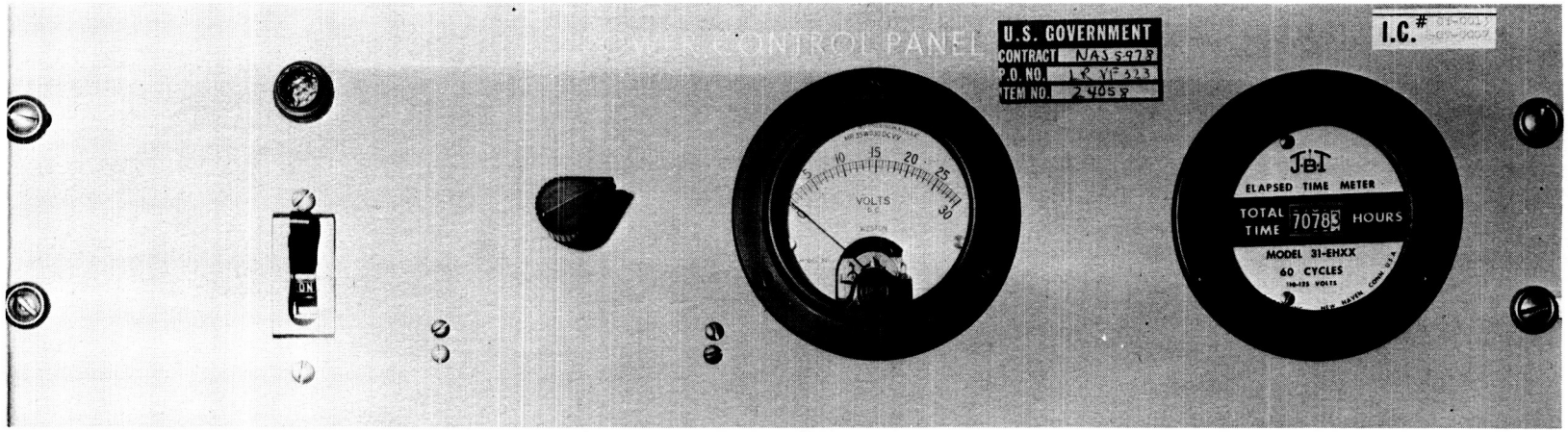


FIGURE I-5 - POWER CONTROL PANEL

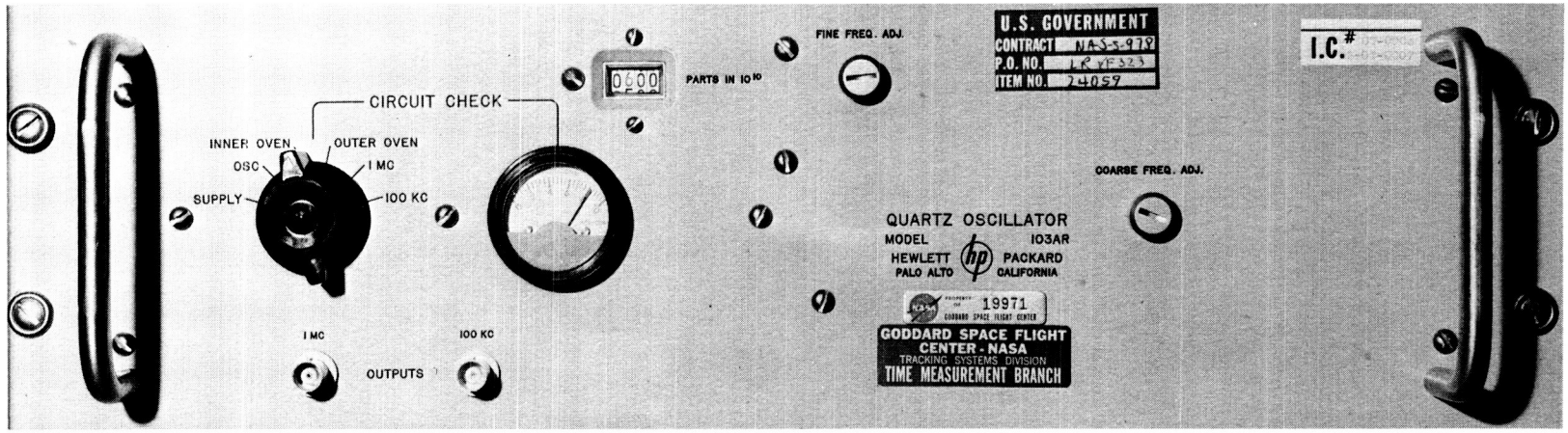


FIGURE I-6 - HP 104 AR QUARTZ OSCILLATOR PANEL

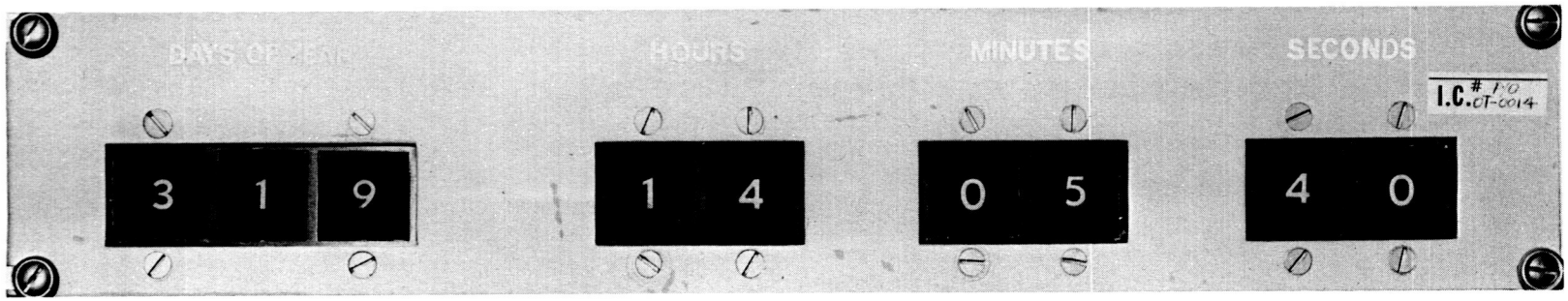


FIGURE 1-7 - DISPLAY PANEL

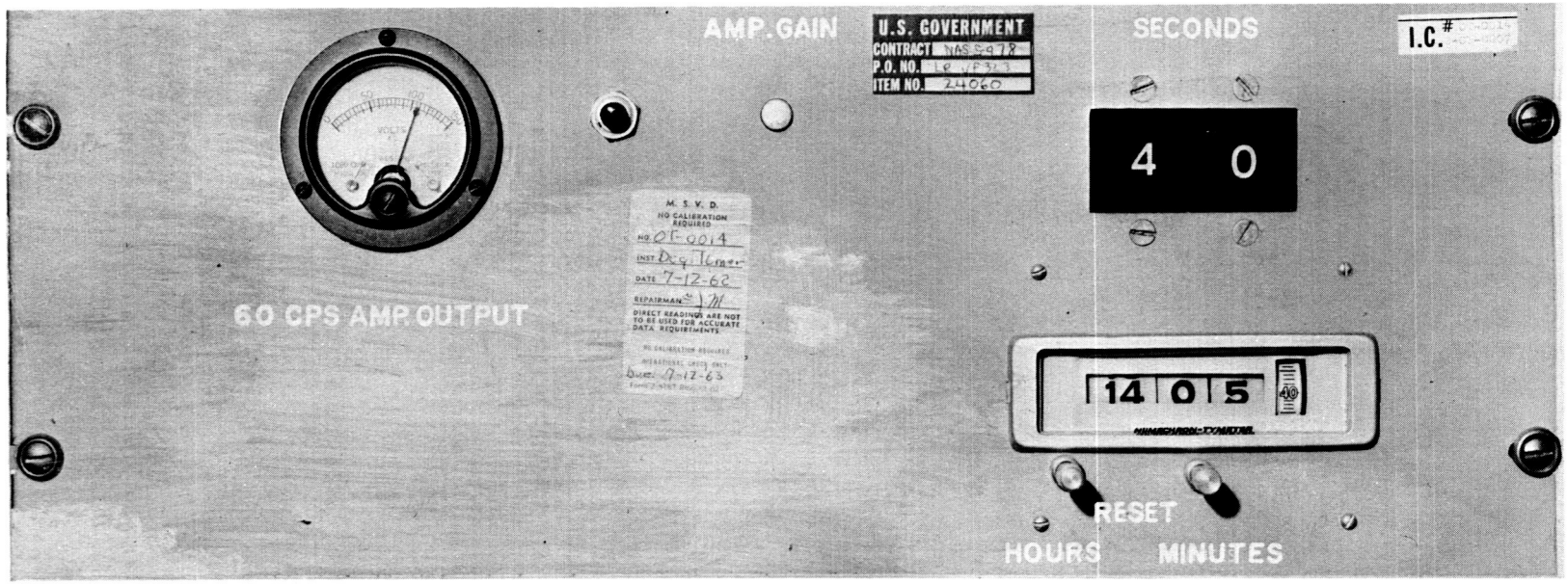


FIGURE I-8 - CLOCK AMPLIFIER PANEL

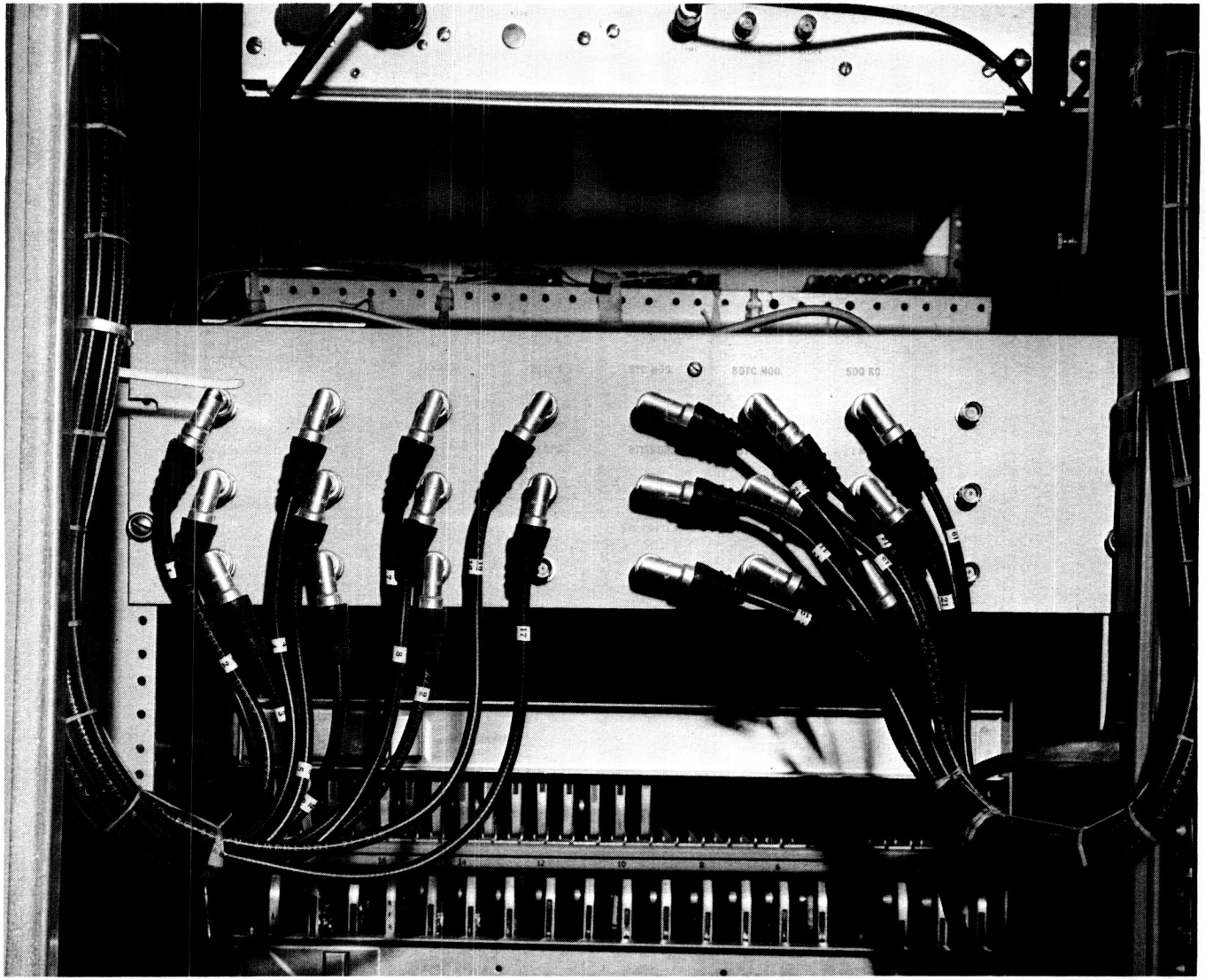


FIGURE I-9 - SIGNAL DISTRIBUTION PANEL (CHASSIS)

7. Converter Panel

The Converter Panel, Figure 1.10, is the seventh panel from the top of the right-hand cabinet. It occupies 7 inches of vertical rack space. The various inputs to and the outputs from this unit are connected to a terminal board mounted on the front of the panel.

8. Emergency Power Transfer Panel

The Emergency Power Transfer Panel, Figure 1.11, is the eight panel from the top of the right-hand cabinet. It occupies 7 inches of vertical rack space.

The units which comprise this panel are mounted on a pull-out rack which provides easy access to the internal adjustment of the emergency power supply.

There are three operating controls on this panel, a "Voltage Monitor" switch and a 0-30-volt d.c. meter for monitoring the various voltages of the emergency power supply, an "AC Power" switch with lamp to indicate "On" conditions, and a "Charge Rate" switch with two lamps to indicate "Fast Charge" conditions or "Normal Charge" conditions.

The "Charge Rate" meter measures the battery charging current or "Load Current."

Located just below this panel is the battery box and the transformer.

9. 305 Tektronic Oscilloscope Panel

The 305 Tektronic Oscilloscope Panel is located at the top of the left-hand cabinet. It occupies 7 inches of vertical rack space. A complete description of this unit can be found in the manufacturer's instruction manual referenced in Table 1.1.

10. Berkeley 905 WWV Receiver

The Berkeley 905 WWV Receiver, Figure 1.12, is the second panel from the top of the left-hand cabinet. It occupies 5 1/4 inches of vertical rack space. A complete description of this unit can be found in the manufacturer's instruction manual referenced in Table 1.1.

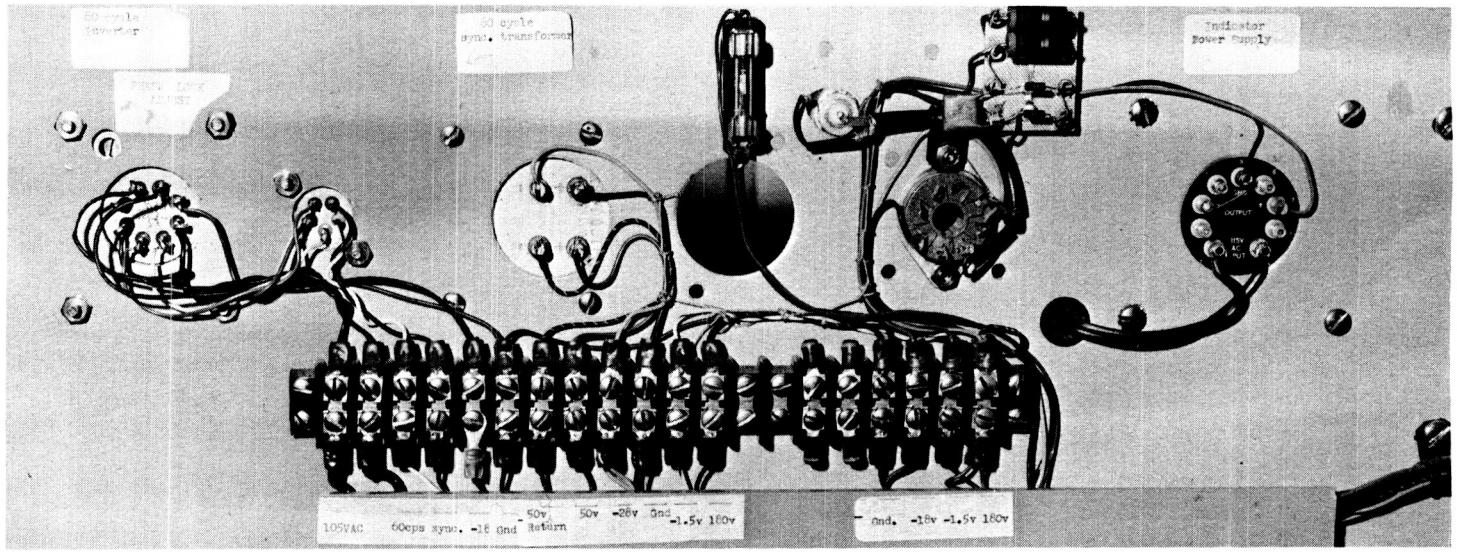


FIGURE I-10 - CONVERTER PANEL

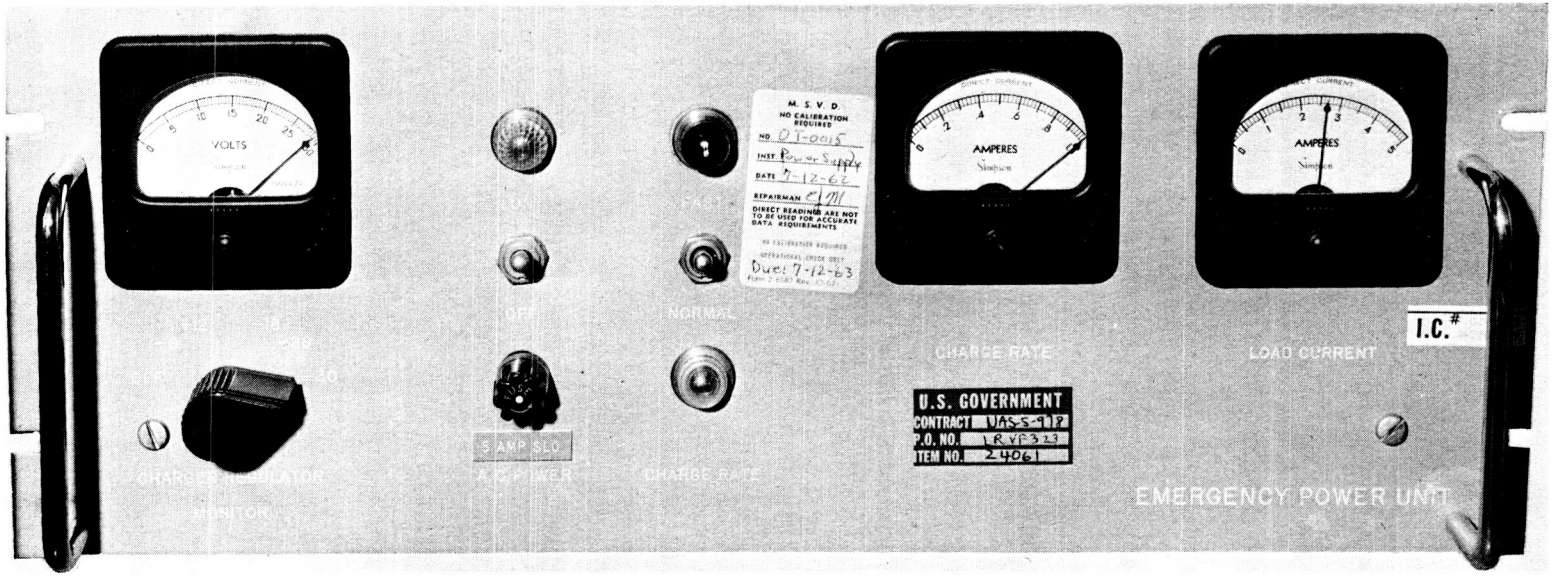


FIGURE I-11 EMERGENCY POWER TRANSFER PANEL

11. Control Panel

The Control Panel, Figure 1.13, is the third panel from the top of the left-hand cabinet. It occupies 7 inches of vertical rack space.

The switches on this panel are grouped according to their use. Their functions are explained below.

Group A

This group of switches is used to synchronize the frequency divider to WWV. Located at the top left of this panel are two switches: "Rate Selector" and "Advance-Retard". These switches are used in the coarse synchronization of the time standard to WWV. Located below the "Rate-Selector" switch is the frequency divider "Reset" switch which is used to reset the seconds and tens of seconds counters of the frequency divider to zero. Located in the center of the panel is the "Phase-Shifter" control which is used for the fine (day-to-day) synchronization of the time standard to WWV.

Group B

This group of switches is used to synchronize the digital clock to WWV. Located in the top right-hand corner of the panel are the Digiswitches. These switches are used to set a predetermined time in the digital clock. Located at the top center of the panel is an "On-Off" switch. When in the "Off" position this switch prevents the 1 PPS signal output of the frequency divider from advancing the digital clock. Located below this switch are the digital clock "Reset" and "Set" switches. The "Reset" switch is used to reset the counters in the digital clock to zero and the "Set" switch is used to set the digital clock to the time determined by the Digiswitches.

Located below the Digiswitches is the "SDTC" indicator light that provides a visual indication of this code.

Located to the right of the "SDTC" indicator are the "Blank Zeros" switch and indicating light.

12. Digital Clock Panel (Chassis)

The Digital Clock Panel is the fourth panel from the top of the left-hand cabinet. It occupies 5 1/4 inches of vertical rack space.

FIGURE I-12 - BECKMAN/BERKELEY WWV RECEIVER

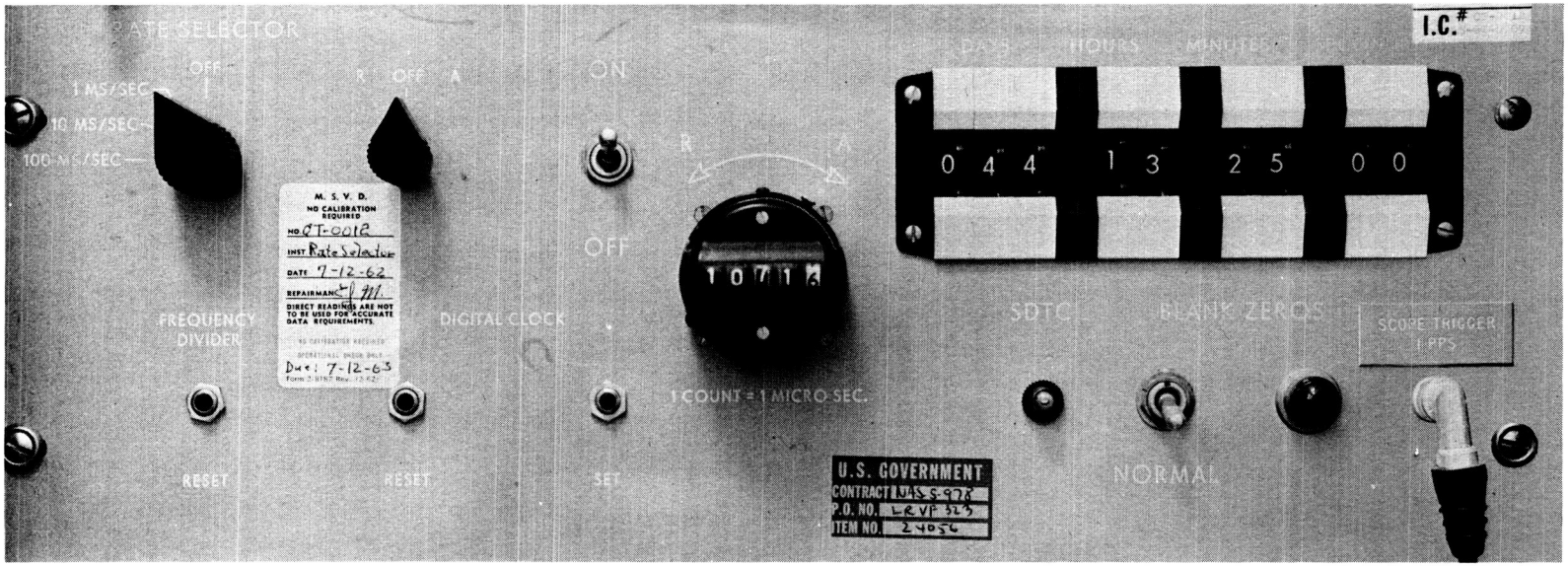


FIGURE I-13 - CONTROL PANEL

The decade counters and all the associated circuitry for the digital clock are housed in this unit. When mounted in the cabinet, this unit is covered with a plain panel.

13. Time Code Generator Panel (Chassis)

The Time Code Generator Panel is the fifth panel from the top of the left-hand cabinet. It occupies 5 1/4 inches of vertical rack space. When mounted in the cabinet, this unit is covered with a plain panel.

14. RP-32 Power Supply Panel

The RP-32 Power Supply Panel is the bottom panel of the left-hand cabinet. For a complete descriptionof this unit see the manufacturer's instruction manual referenced in Table 1.1.

15. Top Panel

The Top Panel, Figure 1.14, is mounted at the top of the right-hand cabinet. This panel contains the various connectors used in connecting the outputs from the time standard to the data acquisition system. The 115-volt 60-cps power is brought in through this panel.

C. Functional Description

All timing signals originate from a highly stable and accurate one-megacycle oscillator. Decade counters are used to provide highly accurate and stable synchronizating pulses and the parallel binary coded decimal time of year information.

Various gating networks and signal conditioning circuits are used to provide the Serial Decimal Time Code (SDTC) and the NASA 1/sec Binary Time Code (BTC).

The time comparison circuits are used in conjunction with the oscilloscope and the WWV receiver to provide a coincident display of the locally generated one-pulse-per-second signal and the WWV time signal (time tick).

Over a period of time, any error of the local one-megacycle oscillator can be observed and measured. Corrections for this frequency error are accomplished by manually readjusting the

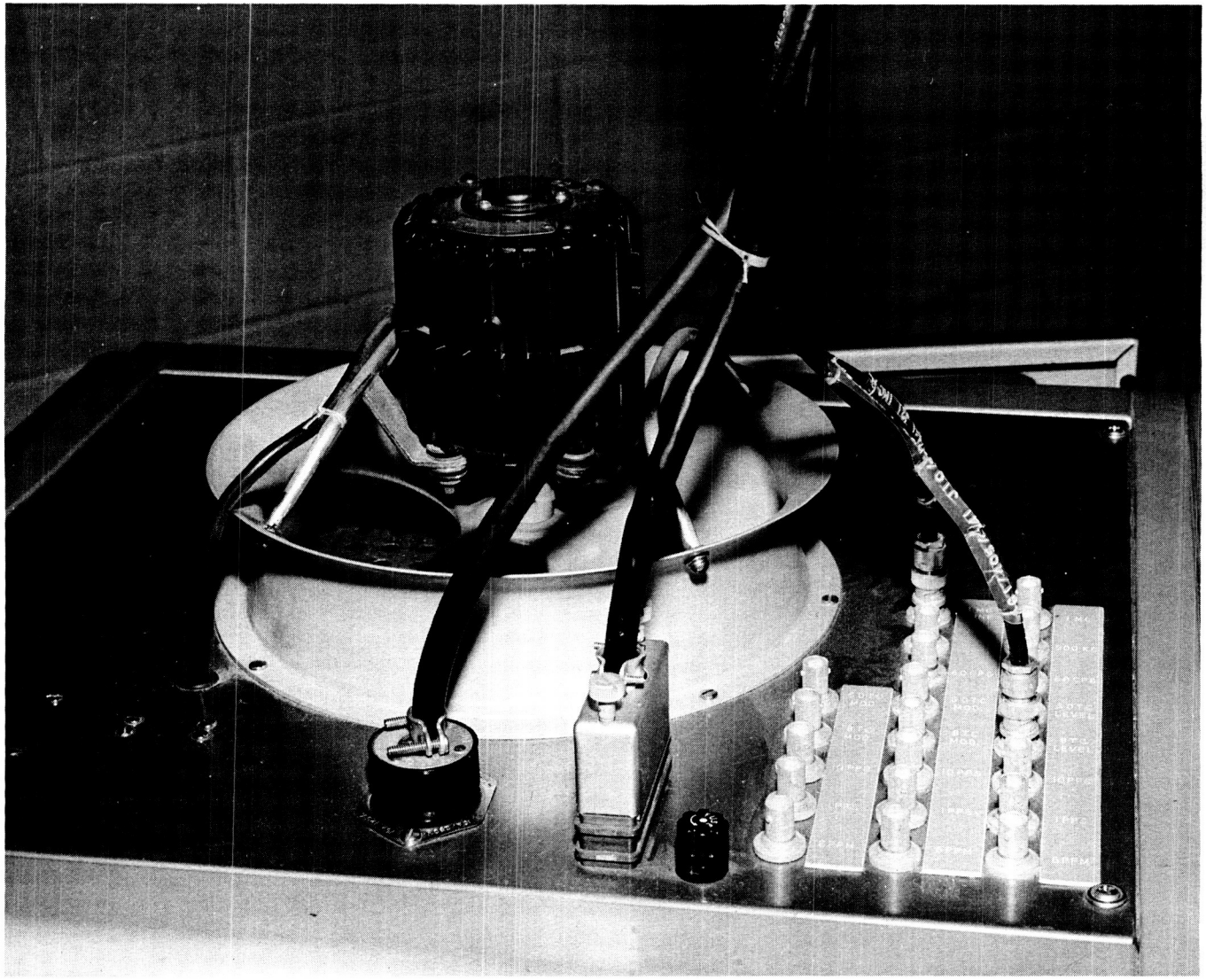


FIGURE I-14 TOP PANEL

frequency of the oscillator.

The following paragraphs present brief functional descriptions of each unit of the time standard. These units are treated in sequence generally following the pattern of signal development.

1. One-Megacycle Oscillator

The one-megacycle oscillator provides a very accurate and stable one-megacycle signal from which all other signals are derived. It also provides a five-megacycle signal with extreme spectral purity for use with the telemetry and tracking receivers.

2. Frequency Divider Unit

The frequency divider accepts the one-megacycle signal from the basic oscillator and, through appropriate decade counters connected in cascade, produces the highly accurate and stable synchronizing pulses for use by the timing system and the data acquisition system.

An important feature of one of the circuits in the frequency divider is the capability of advancing or retarding the 1-pulse-per-second signal in amounts governed by the manual rotation of a resolver. This feature allows for fine synchronization between the timing system and the WWV time signal.

Other circuits located in the Frequency Divider Unit generate a highly stable 60-cps sine wave for operating the panel clock and the advance-retard circuit which permits coarse synchronization to WWV.

3. Digital Clock Unit

The digital clock is used to produce two forms of time signals, the serial decimal time code (SDTC) and the binary time code (BTC).

The input to the digital clock is the highly stable and accurate 1-pulse-per-second signal from the frequency divider and through appropriate decade counters connected in cascade maintains Greenwich mean time (GMT) in days of year, hours, minutes, and seconds. The simultaneous outputs from thirty binary stages represent the 30-bit parallel time-of-year information in a binary coded decimal 1-2-4-8 code.

The outputs from the units-of-seconds counter are applied to a binary-to-decimal decoder which produces five sequential timing pulses. These timing pulses select the time digit that is to be compared in the digital comparator. The output from the digital comparator circuit is gated with the 10-pulse-per-second signal from the frequency divider and produces the serial decimal time code (SDTC).

One of the circuits in the digital clock produces an output pulse once every twenty-four hours to reset the tens of hours and units of hours decade counters to zero at the end of each twenty-four hour period.

Digiswitches are used to preset the Digital Clock to a predetermined time when synchronizing the time standard to WWV.

4. Binary Time Code Generator

The binary time code generator receives the time-of-year information from the digital clock in parallel form and through the use of shift registers produces the NASA 1/sec BTC.

5. Signal Distribution Chassis

The Signal Distribution Chassis receives the signals from the frequency divider, digital clock, and the binary time code generator and distributes these signals to the Top Panel and the time-of-year information to the time-of-year display unit. The Signal Distribution Chassis also serves as a buffer between the input and output circuits and as a shaper for the 100-KC, 50-KC, 5-KC, and 1-KC sine waves.

6. Top Panel

The Top Panel contains the various connectors used in connecting the outputs from the time standard to the data acquisition system.

7. Time-of-Year Display Chassis

The Time-of-Year Display Chassis receives the parallel binary coded decimal time-of-year information from the Signal Distribution Chassis and displays it on nine digital indicating tubes.

8. Emergency Power Supply

The Emergency power supply is a transistorized power supply, battery charger, and battery which is used as a standby

supply and furnishes the necessary power to the frequency divider, the 60-cps panel clock, and the HP 104 AR oscillator when the main supply fails.

9. RP-32 Power Supply Unit

The RP-32 power supply unit is a transistorized power supply that is used to supply power to the digital clock, the binary time code generator, and the Signal Distribution Chassis.

10. Converter Chassis

The Converter Chassis contains the following components:

a. DC-to-DC converter: Sorensen QC28/50/0-5QC converter that is used in the development of the positive 12-volt dc emergency power.

b. ERA Transpac Model TR200M converts the 115-volt ac to 200 volts dc for use by the time comparison circuit, card 16, located in the frequency divider, and 180-volt dc for use by the digital indicator tubes.

c. The IT-226A ERA DC-to-AC converter is operated from the emergency supply and is used to drive the numechron clock. The 60-cps output from the converter is synchronized by the 60-cps signal generated in the frequency divider.

SECTION 2
SYSTEM OPERATION

2.1 GENERAL

This section describes the turn-on procedures and system operational checks for the time standard.

NOTE

Examine all units to see that they are properly mounted in the time standard rack. Inspect all cables to see that they are securely fastened.

2.2 TURN-ON PROCEDURE

The procedure for the application of power to the time standard is as follows:

1. Check to make certain that all switches on the rack are in the "Off" or "Normal" position and that the batteries are disconnected.
2. Connect the time standard to a 115-volt 60-cps power source.
3. Place the "AC Power" switch (15-amp. circuit breaker) located on the Power Control Panel to the "On" position. The light beside the switch will light and the "Elapsed Timing" meter will operate.
4. Turn the "AC Power" switch on the RP-32 power supply to the "On" position.
5. Check to make certain that the switches which control the blowers are in the "On" position.
6. Check the dc voltage outputs from the RP-32 power supply using the "Voltage Monitor" switch and the 0-30 voltmeter located on the Power Control Panel.
7. Turn the "AC Power" switch on the 305 Tektronic Oscilloscope to the "On" position.
8. Turn the "AC Power" switch on the Beckman/Berkeley WWV Receiver to the "On" position.
9. Connect the batteries by inserting the fuse at the rear of this panel.
10. Check to make certain that the "Charge Rate" switch on the Emergency Power Transfer Panel is in the "Normal" position.
11. Turn the "AC Power" switch on the Emergency Power Transfer Panel to the "On" position.
12. Check to make certain that the digital indicators located on

the Display Panel light up. Also check to make certain that the digital indicators which represent the seconds change.

13. Check to make certain that the 60-cps panel clock is running.

14. Check the voltage monitor on the AR 104 oscillator.

2.3 CALIBRATION AND ADJUSTMENT

Allow the equipment to reach operating temperature before proceeding to synchronize the time standard to WWV. This should take about four hours. An initial "aging" period of two to three days should be allowed before any attempt is made to adjust the frequency of the one-megacycle oscillator.

A. Synchronizing the Frequency Divider with WWV

1. Do not change the stable one-megacycle oscillator settings for the initial synchronizing of the frequency divider with WWV. Allow four hours for the oscillator to reach operating temperature after initial turn-on. The oscillator adjustment is described in paragraph 2.4.

2. After a one-minute warmup, turn the "Band Selector" switch on the WWV receiver to the position which gives the strongest signal on the signal strength meter.

3. Rotate the "Gain" control fully clockwise until a switch clicks audibly at the "AGC" position, thus activating the automatic gain control portion of the receiver circuitry.

4. Adjust the "OSC Tuning" control for a maximum reading on the signal strength meter.

5. Adjust the "Audio Gain" for desired volume and oscilloscope amplitude.

6. Adjust "Limiter" control for maximum signal-to-noise ratio. When the WWV filtered tone signal is being received, a constant-amplitude sine wave train with one interruption (second time interval) appears on the oscilloscope screen.

7. The one-second timing pulses (or ticks) transmitted by WWV consist of a 5-millisecond pulse of 1000-cps sine wave with exact time at the positive zero crossing of the first pulse, Figure 2-1.

8. Intervals of one minute are marked by omitting the last tick of each minute and commencing each minute with two ticks separated by 100 milliseconds.

9. Depress the Frequency Divider "Reset" switch located on the Control Panel. This will reset the seconds and tens of seconds decade counters to zero and inhibit the 1-PPS signal.

10. Release the "Reset" switch at the 59th second. The seconds

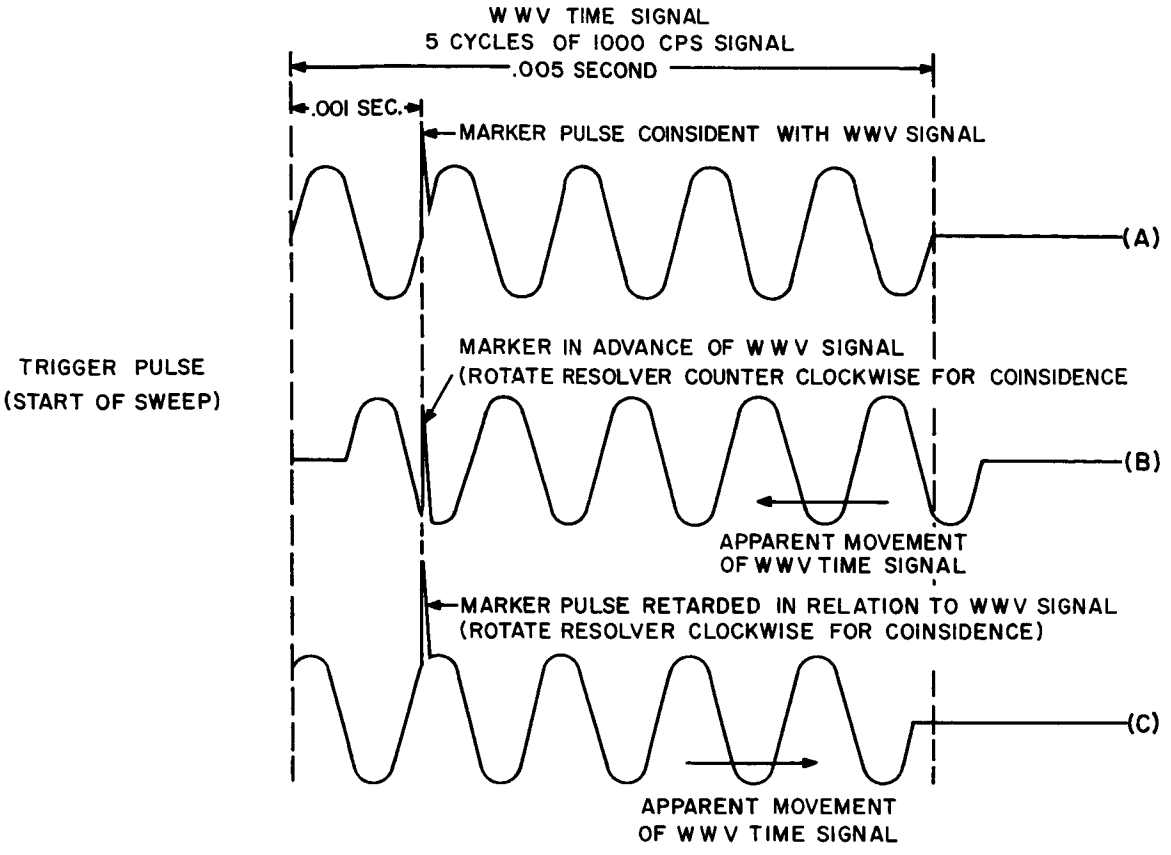
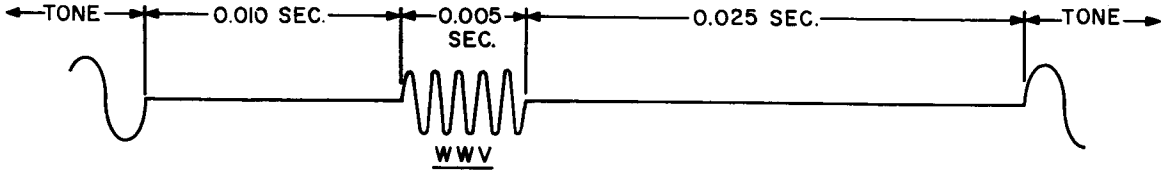
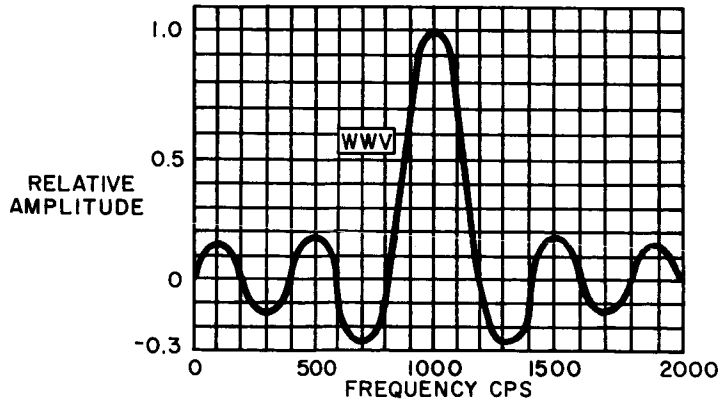


FIGURE 2.1A TIME INTERVAL PULSE WAVEFORM





THE FREQUENCY SPECTRUM OF WWV SECONDS PULSES

THE SPECTRUM IS COMPOSED OF DISCRETE FREQUENCY COMPONENTS AT INTERVALS OF 1.0 CPS. THE WWV PULSE CONSISTS OF FIVE CYCLES OF 1000 CPS.

FIGURE 2.1B WWV AND TIME SET PULSE GENERATOR

and tens-of-seconds decade counters will resume counting the 1-PPS signal.

11. Set the oscilloscope for a sweep rate of 100 ms/cm (1000 ms full scale). Observe the oscilloscope display to determine where the WWV time interval signal occurs with respect to the beginning of the oscilloscope trace.

NOTE

This method of synchronizing the frequency divider to WWV will cause the locally generated time to be fast when compared to the WWV time interval signal. Proper time tick will occur to the right of the scope trigger.

12. Set the "Advance-Retard" switch located on the Control Panel to the "R" position while watching the oscilloscope sweep trace set the "Rate-Selector" switch to the 100 mc/sec position. This will cause the WWV time interval signal to move to the left across the oscilloscope screen at a rate of 100 ms per second.

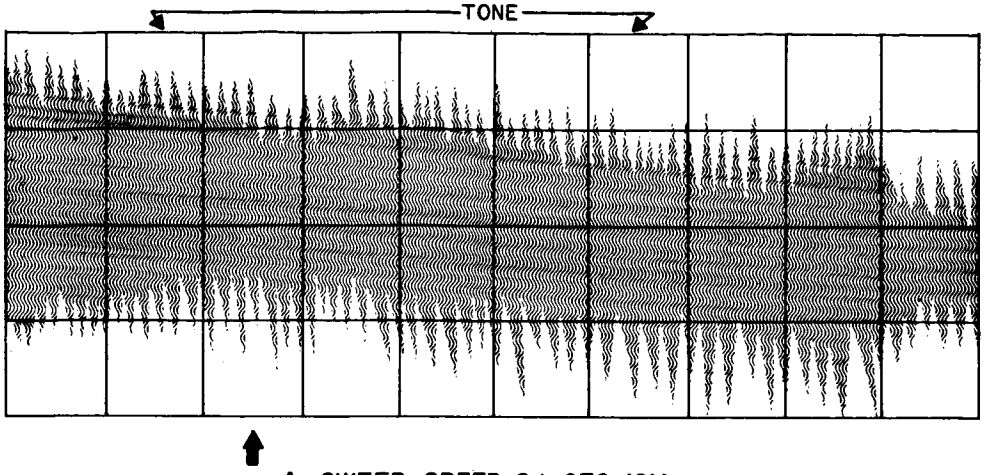
13. When the WWV time interval signal has moved to within 100 ms of the left-hand side of the oscilloscope screen, set the "Rate-Selector" switch to 10 mc/sec position and change the sweep rate of the oscilloscope to 10 ms/cm (100 ms) full scale.

14. When the WWV time interval has moved to within 10 ms of the left-hand side of the oscilloscope screen, set the "Rate-Selector" switch to the 1-ms/sec position and change the sweep rate of the oscilloscope to 1-ms/cm (10 ms full scale).

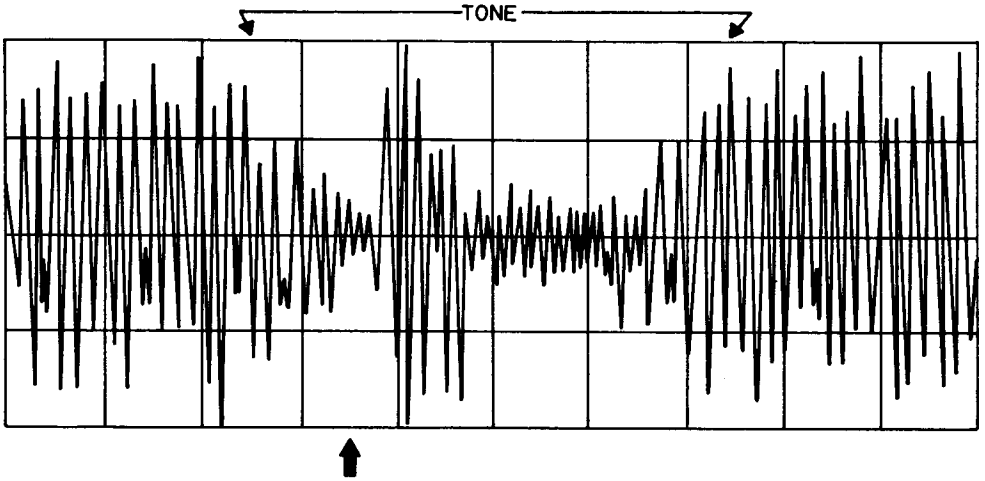
15. When the WWV time interval has moved to within 1 ms of the left-hand side of the oscilloscope screen, turn the "Advance-Retard" switch and the "Rate-Selector" switch to the "Off" position.

16. While watching the seconds and tens-of-seconds indicators, listen for the double tick of the WWV time interval signal (the double tick indicates the beginning of a minute) or the voice announcement of the time to make sure the frequency divider is counting the correct seconds.

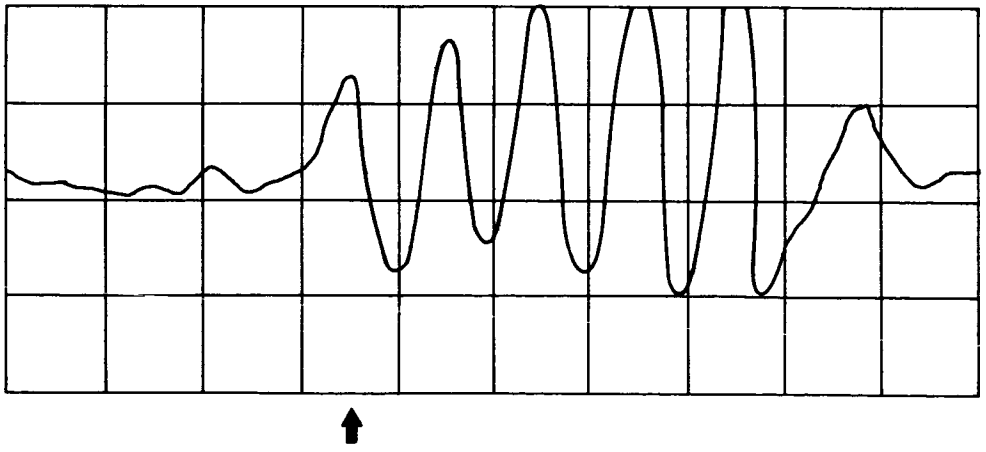
17. Use the "Phase Shifter" control, located on the Control Panel, to obtain a fine adjustment of the synchronization. Synchronization is obtained when the delayed 1 PPS from the time standard and the positive-going zero crossing of the second cycle of the WWV time interval signal occur simultaneously as illustrated in View A of Figure 2.2.



A. SWEEP SPEED 0.1 SEC./CM



B. SWEEP SPEED 10 MCSEC./CM



C. SWEEP SPEED 1 MSEC./CM

NOTE: ARROW POINTS TO LEADING EDGE OF WWV TICK

FIGURE 2.2 TYPICAL WWV WAVEFORM

NOTE

Move the "Phase-Shifter" dial in the advance direction indicated by the letter "A" or in the retard direction indicated by the letter "R". One complete revolution of the dial is equal to 100 microseconds. Log "Phase-Shifter" dial reading, the time of day the adjustment was made, and the oscillator setting for future adjustment.

18. Listen for the next double-time marker signal at the beginning of the next minute. When the first of these two signals occurs, the tens-of-seconds and seconds indicators on the Control Panel should read zero. If this is not indicated, repeat the synchronizing procedure.

NOTE

Site operating procedures may require adjusting the timing equipment to compensate for the transit delay time of WWV signals. Do not compensate for the WWV transit delay time unless it is specifically called out in the station operations plan. After the frequency divider has been adjusted properly, the delay time as given in Table 2.1 may be inserted by advancing the resolver. The resolver must be rotated ten times for each millisecond's delay.

TABLE 2.1
TRANSIT TIME DELAY OF THE WWV TIMING SIGNALS

NO.	STATION	DELAY (MSEC.)
1.	Fairbanks (College), Alaska	27.4
2.	Blossom Point, Maryland	0.5
3.	Ft. Myers, Florida	5.8
4.	E. Grand Forks, Minn.	7.2
5.	Hartebeeshoek, S. Africa	45.7
6.	Lima, Peru	20.2
7.	Goldstone Lake, California	12.6
8.	St. Johns, Newfoundland	8.1
9.	Island Lagoon, Australia	59.1
10.	Quito, Ecuador	16.1
11.	Rosman, N.C.	3.6
12.	Santiago, Chile	28.7
13.	Fairbanks (Ulaska), Alaska	27.4
14.	Winkfield, England	20.8

B. Synchronizing the Digital Clock with WWV

1. Place the "On-Off" switch on the Control Panel to the "Off" position. This will inhibit the 1 PPS from the frequency divider.

2. Use the "Digital Clock Reset" switch located on the Control Panel and reset the digital clock to zero.

3. Set the day-of-year number on the "Digiswitches" to the day of the year. The day of the year may be obtained from a desk calendar.

4. Listen to WWV for a voice announcement of the time of day.

5. Set the hours on the "Digiswitches" to the announced time.

6. Set the minutes on the "Digiswitches" in advance of the announced time. Set the seconds to zero.

7. Set the information contained on the "Digiswitches" in the digital clock by depressing the "Digital Clock Set" switch.

8. Listen to the received WWV time interval signals. When the received time becomes equal to the preset time in the digital clock, turn the "On-Off" switch to the "On" position. The digital clock should now be synchronized with WWV. As an aid, observe the seconds indicator of the frequency divider and turn the switch to "On" when it reads 00.

9. Recheck the time standard by listening to a voice announcement of the WWV time. The announced time and the time displayed by the digital clock indicators should be the same.

NOTE

When using the WWV voice announcement to set the digital clock, conversion to Greenwich mean time must be accomplished.

C. Synchronizing the Panel Clock with the Digital Clock

1. Depress and hold the "Time Set" switch. This removes the power from the clock motor.

2. Using the "Hours and Minutes Set" control, set the clock one minute in advance of the time displayed by the digital clock.

3. Observe the time displayed on the frequency-divider seconds and tens-of-seconds indicators, and when this time becomes equal to the time preset in the clock release the "Time Set" switch.

4. Synchronize the two clocks closely by momentarily closing the "Time Set" switch.

NOTE

Because of the inertia of the clock motor, it

may be necessary to determine experimentally when to release the "Time Set" switch in order to start the clock at the right time.

D. Adjustment of the One-Megacycle Basic Oscillator

1. General

To obtain the accuracy demanded of the data-acquisition-system timing system, it is necessary to assure that the basic oscillator is operating at the correct frequency and that it has the stability which will maintain timing signals in close synchronization with radio station WWV.

After the timing system has been placed into operation and a stabilizing period of about four days has elapsed, it may be necessary to adjust the frequency of the oscillator. The following procedures should be followed when this adjustment is necessary.

During the stabilization period make a time comparison with WWV every two to four hours and tabulate the "Phase-Shifter" dial readings. The average fractional error in frequency of the oscillator is equal to the fractional time error (Phase-Shifter dial reading) and is given by:

$$\frac{\Delta f}{f} = \frac{t_2 - t_1}{T} \quad \text{(For plotting purposes only)} \qquad \text{Eq. 2.1}$$

Where $\frac{\Delta f}{f}$ = average frequency error

t_1 = final time comparison measurement (Phase-Shifter dial reading)

t_2 = final time comparison measurement (Phase-Shifter dial reading)

T = elapsed time between readings.

NOTE

Do not adjust the frequency of the oscillator during the stabilization period.

After the oscillator has stabilized, make a time comparison measurement and record the "Phase Shifter" dial reading in

microseconds as t_1. At the end of a 24-hour period make another time comparison reading and record the "Phase Shifter" dial reading in microseconds as t_2. Subtract t_1 from t_2. If the difference between these readings is less than 1,000 microseconds do not adjust the oscillator frequency. Continue the time comparison measurements every 24 hours until the difference between t_1 and t_2 is 1,000 microseconds or greater.

Use the following formula to determine the amount by which the oscillator frequency should be adjusted:

$$\frac{\Delta f}{f} = \frac{t_2 - t_1}{\text{days}} \times \frac{1 \text{ day}}{8.64 \times 10^{10}} \qquad \text{Eq. 2.2}$$

Example 1: The initial "Phase Shifter" dial reading t_1 is 36,000 microseconds and the second "Phase Shifter" dial reading t_2 is 37,000 microseconds. The time that has elapsed between the two readings is 10 days; then:

$$\frac{\Delta f}{f} = \frac{t_2 - t_1}{T \text{ (days)}} \times \frac{1 \text{ day}}{8.64 \times 10^{10}}$$

$$= \frac{37,000-36,000}{10} \times \frac{1}{8.64 \times 10^{10}}$$

$$= \frac{1000 \text{ microseconds}}{10} \times \frac{1}{8.64 \times 10^{10}} = \frac{1000}{86.4 \times 10^{10}}$$

$$= 11.6 \text{ parts in } 10^{10} \text{ of } 0.0011 \text{ CPS}$$

This means that the oscillator frequency has decreased, causing the clock to lose time. Therefore, the frequency of the oscillator must be increased by 11.6 parts in 10^{10} or .0011 CPS.

Example 2: The initial "Phase Shifter" dial reading t_1 is 36,000 microseconds, and the second "Phase Shifter" dial reading t_2 is 35,000 microseconds. The time that has elapsed between the two readings is 10 days; then:

$$\frac{\Delta f}{f} = \frac{35,000-36,000}{10} \times \frac{1}{8.64 \times 10^{10}}$$

$$= \frac{-1000 \text{ microseconds}}{10} \times \frac{1}{8.64 \times 10^{10}} = \frac{-1000}{86.4 \times 10^{10}}$$

$$= -11.6 \text{ parts in } 10^{10} \text{ or } -0.0011 \text{ CPS}$$

This means that the oscillator frequency has increased, causing the clock to gain time. Therefore, the frequency of the oscillator must be lowered by 11.6 parts in 10^{10} or .0011 CPS.

The use of Table 2.2 will eliminate the routine daily frequency-error computation. In order to use this table, a daily time comparison must be made and the value of the "Phase-Shifter" dial reading tabulated.

When it is determined by the application of the tabulated information in Table 2.2 that the oscillator requires frequency correction, the following procedures should be followed:

2. Adjustment of the HP 104 AR Quartz Oscillator

a. Fine Frequency Adjust

Remove the "Fine Freq. Adj." threaded plug and adjust the "Fine Freq. Adj." until the change in the parts in the 10^{10} counter equals the parts in 10^{10} determined from the information tabulated in Table 2.2.

The counter is usable only to 600. After 600, the hundreds digit appears in red. When the red number is reached, it becomes necessary to use the "Coarse Freq. Adj."

b. Coarse Frequency Adjust

If it becomes necessary to use the Coarse Freq. Adj., proceed as follows:

Remove the Coarse Freq. Adj. threaded plug on the front panel. The Coarse Freq. Adj. gives 10,000 parts in 10^{10} change for approximately 180-degree rotation; thus, 18-degree rotation will give approximately 1000 parts in 10^{10} change and 4 1/2 degrees will give approximately 250 parts in 10^{10} change.

Remove the Fine Freq. Adj. threaded plug and adjust the Fine Freq. Adj. until the parts in the 10^{10} counter indicate 300.

Adjust the Coarse Freq. Adj. clockwise 4 1/2 degrees for a frequency lower by 250 parts in 10^{10}.

Adjustment is made by inserting a screwdriver in the Coarse

TABLE 2.2 FREQUENCY ERROR

$t_2 - t_1$ in micro-seconds	PARTS IN 10^{10} ELAPSED DAYS									
	1	2	3	4	5	6	7	8	9	10
10	1.1	0.6	0.4	0.3	0.2	0.2	0.2	0.1	0.1	0.1
20	2.3	1.1	0.7	0.6	0.5	0.4	0.3	0.3	0.3	0.2
30	3.5	1.7	1.1	0.9	0.7	0.6	0.5	0.4	0.4	0.3
40	4.6	2.3	1.5	1.1	0.9	0.8	0.7	0.6	0.5	0.5
50	5.8	2.9	1.9	1.4	1.1	1.0	0.8	0.7	0.6	0.6
60	6.9	3.5	2.3	1.7	1.4	1.1	1.0	0.9	0.8	0.7
70	8.1	4.1	2.7	1.8	1.6	1.3	1.1	1.0	0.9	0.8
80	9.2	4.6	3.1	2.3	1.8	1.5	1.3	1.1	1.1	0.9
90	10.4	5.2	3.5	2.6	2.1	1.7	1.5	1.3	1.1	1.0
100	11.6	5.8	3.9	2.9	2.3	1.9	1.6	1.4	1.3	1.1
200	23.1	11.6	7.7	5.8	4.6	3.8	3.3	2.9	2.6	2.3
300	34.7	17.4	11.6	8.7	6.9	5.8	4.9	4.4	3.9	3.5
400	46.2	23.1	15.4	11.6	9.2	7.7	6.6	5.8	5.2	4.6
500	57.9	28.9	19.3	14.5	11.6	9.6	8.3	7.2	6.5	5.8
600	69.4	34.7	23.1	17.4	13.9	11.6	10.0	8.7	7.7	7.0
700	81.0	40.6	27.0	18.3	16.2	13.4	11.6	10.2	9.0	8.1
800	92.6	46.3	30.9	23.1	18.5	15.4	13.3	11.6	10.1	9.3
900	104.2	52.2	34.7	26.1	20.8	17.3	14.9	13.1	11.6	10.4
1000	115.7	57.9	38.6	28.9	23.1	19.3	16.5	14.5	12.9	11.6
2000	231.5	115.7	77.2	57.9	46.3	38.6	33.2	28.9	25.8	23.1
3000	347.2	174.0	115.7	87.0	69.3	57.9	49.8	43.5	38.7	34.8
4000	463.0	231.5	154.0	115.7	92.6	76.8	66.4	57.9	51.6	46.4
5000	578.7	289.3	193.0	144.7	115.7	96.0	83.0	72.5	64.5	57.9
6000	694.4	347.2	231.5	174.0	138.6	115.7	99.6	87.0	77.4	69.6
7000	810.2	406.0	270.0	183.0	161.7	134.3	115.7	101.5	90.3	81.2
8000	925.9	463.0	309.8	231.5	184.8	153.6	132.8	115.7	101.2	92.8
9000	1041.7	522.0	347.2	261.0	208.8	174.8	149.4	130.5	115.7	104.4
10000	1157.4	578.7	385.8	289.3	231.5	192.9	165.3	144.7	128.6	115.7

Freq. Adj., pressing in and turning the screwdriver until the outer shaft becomes engaged with the Coarse Freq. Adj. capacitor shaft. Then adjust as needed.

Replace the Fine Freq. and Coarse Freq. Adj. threaded plugs.

The accuracy of the frequency adjustment can be determined when the next time comparison measurement is made. Use the average of several time comparison measurements taken several days apart to adjust any error out of the oscillator.

c. Alternate Method of Adjusting the HP 104 AR Quartz Oscillator

1. Connect the 1MC output of the HP 104 AR oscillator to the horizontal input of the Tecktronic 503 oscilloscope and an external stable oscillator to the vertical input.

2. Adjust the external oscillator until the Lissojoue pattern appearing on the scope rotates once every 150-200 seconds ($\pm$ 50 to 70 x 10^{-9}).

3. Change the HP 104 oscillator fine frequency dial from 600 to 100 or 0 to 500; then change the coarse frequency adjust until the Lissojoue pattern rotates once every 100-200 seconds.

NOTE

This method will allow the HP 104 AR oscillator to be set to an accuracy of approximately 1 x 10^{-8}.

4. Make a time comparison with the WWV time interval as outlined in paragraph 2.3.

3. Adjustment of the Hermes 101C Ultra Stable Oscillator

Each division of the Fine Freq. control dial represents a frequency change of one part in 10^9. The number of divisions by which the dial is to be changed can be found from the tabulated information listed in Table 2.2.

The Coarse Freq. control permits the oscillator to be adjusted over a range of 1.0 cycle per second in steps of 0.1 cycle per second. This makes the relationship between the Coarse Freq. and

Fine Freq. controls 100 to 1. Consequently, when a frequency correction of more than 100 fine-frequency control divisions is necessary, the Coarse Freq. control setting should be adjusted to make this compensation.

An additional fine-frequency vernier scale is imprinted on the face of the Fine Freq. control knob. This 0-100 scale is to be used for logging purpose only.

Both the Coarse and Fine Freq. control dials are marked with positive (+) and negative (-) numbers. When the timing signal exceeds those from WWV, a negative (or decreasing positive) correction will be necessary. For example, if the "Phase Shifter" dial is turned in a counterclockwise direction to obtain coincidence, it is indicative of the oscillator frequency being greater than one megacycle. A negative correction should then be inserted into the frequency controls, the amount of correction having been determined from Table 2.2.

A positive (or decreasing negative) correction is inserted if the timing signal lags the WWV time.

2.4 OPERATIONAL CHECKS

A. General

The following paragraphs describe the checks to be performed to determine if the time standard system is functioning properly. Detailed procedures for checking out the standard units can be found in the manufacturer's instruction manual referenced in Table 1.1.

1. Connect the time standard to 115-volt, 60-cps power source.
2. Listen for the operation of the rack fans.
3. Turn the "AC Power" switch, located on the Power Control Panel, to the "On" position. The "AC Power" indicating light should light and the "Elapse Timing" meter should operate.
4. Turn the "AC Power" switch on each unit to the "On" position. The "AC Power" indicating light should light.
5. Use the "DC Voltmeter" select switch and associated "DC Meter" located on the Power Control Panel and check the DC voltage. These voltages should read: 12VDC
   - 6VDC
   -18VDC

6. Connect the batteries and set the "Charge Rate" meter on the Emergency Power Panel to the "Normal" position. The "Charge Rate" meter should read approximately 100 ma.

7. Use the "Charger Regulator Voltage Monitor" switch and check the voltages on the Emergency Power Supply. These voltages should read:

- 6VDC	-28VDC
+12VDC	-30VDC (Adjust and check frequently.)
-18VDC	

8. Recheck all ac and dc power indicating lights.

9. Check alignment of local marker pulse and WWV time interval signal for drift.

10. Check that the times displayed on the seconds and tens of seconds indicators located on the Control Panel display the correct seconds.

11. Check that the digital clock and the panel clock agree with the time announced by WWV.

12. Check the serial decimal time on a strip recorder. See that it agrees with the time displayed on the digital clock.

13. Check for the presence of the following signals at the Top Panel:

a. 1-mc 6-4 pulse
b. 1-mc sine wave
c. 500-KC Sq. Wave
d. SDTC level shift & modulated
e. BTC level shift & modulated
f. 10 PPS
g. 1 PPS
h. 6 PPM
i. 30-Bit parallel binary coded decimal
j. 60 cps

B. Emergency Power

1. Certain units of the timing system operate continuously from the emergency power supply. Should a power failure occur, a nickel-cadmium battery connected to the circuit will maintain basic timing signals for a period of approximately two to three hours. No switching action is necessary for the emergency operation, but after restoration of power the digital clock will require resynchronization as outlined in paragraph 2.3B, except that the hours and minutes may be taken from the numechron panel clock and the seconds from the frequency-divider seconds indicators.

2. The battery should be disconnected by removing the fuse if the ac power failure exceeds three hours. A complete resynchronization and adjustment of the timing system is required whenever the batteries are disconnected during an ac power failure.

SECTION 3
THEORY OF OPERATION

3.1 GENERAL

A. Purpose

The detailed theory of operation of the time standard is presented in this section. Some of the units used are standard items and the detailed theory of operation of these units is contained in the applicable manufacturer's instruction manual referenced in Table 1.1.

The theory of operation contained herein applies only to the units designed specifically for use by the time standard, except where information on the standard items is necessary for a complete understanding of the timing system.

B. Block Diagram Descrption of the Time Standard (Fig. 3.1)

The time standard performs two very important functions; it develops accurate and highly stable timing signals and it synchronizes these signals with Radio Station WWV or to a time standard radio broadcast.

The various outputs are grouped according to their use and are described below:

a. Synchronizing pulses
b. Binary coded decimal time (BCD) in parallel and serial form
c. Serial decimal time code (S.D.T.C.)
d. 60-cycle-per-second sine wave

The frequency divider receives the accurate and highly stable one-megacycle signal from the stable oscillator and produces a 60-cycle sine wave and synchronizing pulse having the following recurrence rates: 1-megacycle 6-4 rectangular wave, 500,000 PPS, 100,000 PPS, 10,000 PPS, 1,000 PPS, 100 PPS, 10 PPS, 1 PPS, and 6 PPM.

The digital clock receives the 1 PPS, 10 PPS, and 10,000 PPS from the frequency divider and produces the binary coded decimal time of the year in parallel form and the serial decimal time code.

The Binary Time Code Generator receives the Binary Coded Decimal Time of year from the Digital Clock, the 1000 PPS, 100 PPS, 10 PPS, 5 PPS, and 1 PPS from the Frequency Divider, and produces the NASA 1/sec BTC.

C. Computer Control Company, Inc., S-PAC Digital Modules

The Frequency Divider, the Digital Clock, the Binary Time Code Generator, and the Signal Distribution Panel all utilize S-PAC Digital Modules. Familiarity with the theory of operation of these modules is essential in order to understand the operation of the units which utilize them. The manufacturer's instruction manual contains information on the operation and maintenance of these units.

D. Counter Pac, Model BC-30

The Counter Pac, Model BC-30, is a general-purpose plug-in type electronic counter which may be wired for binary or binary-coded-decimal (BCD) operation. Internal gating allows 5-4-2-1 BCD counting as well as divide-by-ten, divide-by-six, and other feedback counting modes.

The following paragraphs describe the operation of the BC-30 Counter Pac connected in divide-by-ten and divide-by-six configurations.

(1) Divide-By-Ten Circuit

The operation of four binaries connected in the Binary Count Mode is described with the aid of the S-PAC Instruction Manual. In the diagram the waveforms are the dc potentials at the output from each binary. Waveforms are oriented in relation to the frequency applied to the input.

Reading from left to right, each up-going line is a positive-going pulse (in this case, from negative six volts to ground) which causes the binary to switch its state. Each down-going line (from ground to a negative six volts) has no effect on the binary. As shown, one output is obtained after a resultant ratio of sixteen input pulses.

Such a system requires 4 indicators, one indicator per bit for the readout. This is a complex system to read if more than one counter is used.

A more convenient indicating system is obtained when the

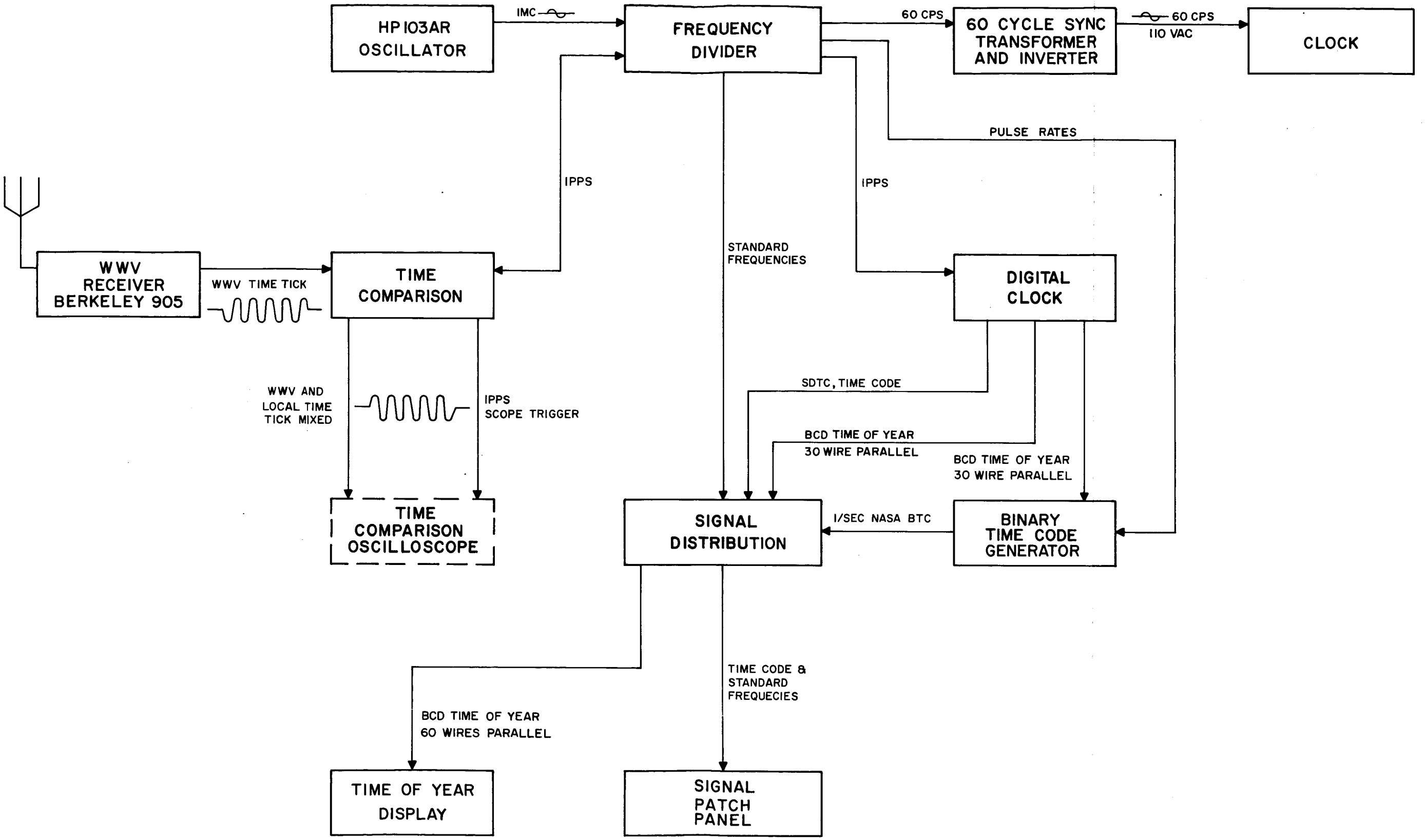


FIGURE 3.1 TIME STANDARD, FUNCTIONAL BLOCK DIAGRAM

division ratio is made to be ten instead of sixteen. The readout can then be a direct-reading decimal number from "0" to "9" with additional counters placed one beside the other. Such a system is shown in the Binary Count Mode.

The waveforms obtained from the divide-by-ten configuration is shown at the bottom of the Binary Count Mode Figure. These waveforms possess the same characteristics as the waveforms explained above.

In the following discussion it is assumed that, initially, all binaries are in the "Zero" state. That is, the true output (pins 20, 27, 18, and 6) from each binary is at ground potential (zero volt).

The second binary stage has a gated complement input. When either of the inputs is at "One" (negative six volts) the gate is enabled and a positive transition at the other input will cause the binary to change its state. However, when one of the inputs is at "Zero" (ground potential) the gate is inhibited and a positive transition at the other input has no effect on the binary. The fourth binary has a gated A.C. reset input. A positive transition applied to either input when the binary is in the set (zero) state resets the stage to the "One" state.

The output from pin 20 of the first binary is utilized as one of the gate inputs to both the second and fourth binaries. The other gate input to the second binary is the output from pin 9 (Reset Output) of the fourth binary. The output from pin 6 (Set Output) of the fourth binary is fedback as the other gate input to the fourth binary.

The first eight input pulses cause the circuit to operate as a straight binary counter. The eighth pulse, however, causes the fourth binary to change its state. The output from pin 9 which was at "one" (negative six volts) now becomes a "Zero" (ground potential) inhibiting the input to the second binary. The output from pin 6 which was at "Zero" (ground potential) now becomes a "One" (negative six volts), enabling the gated input to the fourth binary.

The ninth input causes the first binary to change its state. The output of the first binary (pin 20), which is a negative transition, has no effect on the other binaries.

The tenth input pulse will cause the first binary to again change its state. The positive transition occurring at the output (pin 20) will

have no effect on the second binary because the input gate is inhibited. This positive transition, however, will cause the fourth binary to change its state. Therefore, an output will be obtained after a resultant ratio of ten input pulses.

(2) Divide-By-Six Circuit

The BC-30 Counter Pac is shown in the S-PAC Instruction Manual arranged in a Divide-By-Six configuration. The operation of this circuit is the same as that described for the divide-by-ten circuit except that the third binary is not used.

In this circuit arrangement, one output pulse is obtained after a resultant ratio of six input pulses.

E. Diode Pac, Model DC-30

The Diode Pac, Model DC-30,contains one 2-input NAND gate, five 3-diode clusters, and two 2-diode clusters. The DC-30 NAND gate can be expanded by adding the diode clusters, or the diode clusters may be used to expand the inputs to other S-PAC circuits.

The NAND gate consists of a 2-input gate, followed by a transistor inverter amplifier. When all inputs are at "One" (negative six volts), the gate turns the transistor on and the output is clamped through the transistor to zero volt. When any input goes to zero volt, the transistor is turned off and the output falls to the clamp voltage of negative six volts.

F. NAND Pac, Model DI-30

The NAND Pac, Model DI-30,consists of eight 2-input gates, followed by a transistor inverter amplifier. When all inputs are One (negative six volts), the gate turns the transistor on and the output is clamped through the transistor to zero volts. When any input goes to Zero (zero volt or ground) the transistor is turned off and the output falls to the clamp voltage of negative six volts.

G. Delay Multivibrator/Pulse Shaper Pac, Model DM-30

The Delay Multivibrator/Pulse Shaper Pac, Model DM-30, contains three independent and identical one-shot multivibrators capable of generating pulses in a variety of widths.

Each DM-30 circuit consists of a single input gate (which may be expanded to ten) which is ac-coupled to a monostable multivibrator. The delay cycle is initiated by a positive-going transition at the input.

Pulse width is controlled by connecting the appropriate capacitors to the delay mode. Two or more internally provided capacitors may be connected simultaneously and the resulting pulse has a width equal to the sum of the pulse widths indicated on the block diagram. Other delay times may be obtained by connecting external capacitors across the delay and external delay mode.

H. Adjustable Delay Multivibrator Pac, Model DM-30A

The Adjustable Delay Multivibrator Pac, Model DM-30A, contains three independent and identical variable one-shot multivibrators. The delays available from each circuit are nominally the same as the DM-30. Three potentiometers are mounted on the DM-30A to allow independent pulse-width variation of each circuit.

I. Gate Pac, Model DN-30

The Gate Pac, Model DN-30,contains four 2-input NAND gates, two 3-diode clusters, and 2-diode clusters. The diode clusters may be used to expand the number of inputs.

Each NAND gate performs the NAND function for negative voltage logic (One = negative six volts) or the NOR function for positive voltage logic (One = zero volt).

When all the inputs are at One (in this case negative six volts) the gate turns the transistor on and the output is clamped through the transistor to zero volt. When any input goes to Zero (zero volt) the transistor is turned off and the output falls to the clamp voltage of negative six volts.

The diode clusters may be wired to the mode input of any S-PAC module for expansion of its inputs up to a maximum of 10.

J. Master Clock Pac, Model MC-30

The Master Clock Pac, MC-30,contains a crystal-controlled oscillator, a level restorer, a pulse shaper and a pulse amplifier.

The frequency-generating section of the MC-30 is a series-turned, 1-megacycle crystal oscillator. However, for use in the Time Standard, the crystal has been removed and the MC-30 is externally driven from the HP 104 AR basic oscillator, with the first stage acting as a series-turned amplifier. Following the amplifier is an inverter circuit which clamps the amplifier output to zero volt (ground) and to a negative six volts.

The pulse shaper is a one-shot multivibrator circuit. This circuit is followed by a pulse-amplifier stage.

K. Power Amplifier Pac Model PA-30

The Power Amplifier Pac, Model PA-30, consists of a single input gate (expandable to 10 inputs) followed by a dual power inverter amplifier. When all inputs are at One (negative six volts), the gate turns the two output transistors on and each output is clamped through a transistor to zero volt. When any input goes to Zero (zero volt), all but one transistor is turned off. This transistor clamps outputs through isolating diodes to a negative six volts.

L. Shift Register Pac, Model SR-30

The Shift Register Pac, Model SR-30, contains four prewired stages capable of operating in serial-parallel, parallel-serial, and serial-serial modes.

The basic circuit of each stage is functionally the same as that of the UF-30 (see N below) except for the addition of the shift gating circuit.

The D. C. Set and reset inputs are used to preset the register to a desired condition. The common reset input is direct-coupled to the reset side of each stage, allowing the four stages to be cleared simultaneously by a single positive-going signal.

M. Schmitt Trigger Pac, Model ST-30

The Schmitt Trigger Pac, Model ST-30, contains two identical and independent Schmitt Trigger circuits. These circuits are regenerative bistable circuits whose operation depends on the input voltage. The shape of the output does not depend on the shape of the input signal.

Transistors Q1 and Q2 comprise a conventional Schmitt Trigger circuit. Transistor Q5 connected to the emitters of both Q1 and Q2 insures that a constant current is switched between Q1 and Q2. Emitter follower Q4 and its associated circuit provides the means of varying the threshold of the Schmitt Trigger. Transistor Q3 is an inverter, whose output is S-PAC compatible in voltage levels and transistion time.

N. Universal Flip-Flop Pac, Model UF-30

The Universal Flip-Flop, Model UF-30, contains two identical, independent flip-flops. When all D. C. inputs are at One (negative six volts) the flip-flop assumes one of its bi stable states. Applying a Zero (zero volt) to a D. C. set causes the flip-flop to assume the set or reset stage, respectively.

The A. C. set (reset) input and associated level control from a two-input gate which, when activated, causes the flip-flop to assume the set (reset) state. The change of the set stage of the flip-flop results from applying a positive-going six-volt step on the AC. set (reset) input with the level control input at ground. The control input conditions are such that if a One (negative six volts) control signal is applied, the differentiated step is blocked, but if Zero (zero volt) is applied, the differentiated step is gated into the flip-flop and causes the change of state.

3.2 FREQUENCY DIVIDER

A. General

The Frequency Divider accepts the one-megacycle sine wave from the basic oscillator and counts it down to pulsed output signals of 500,000 PPS, 100,000 PPS, 1,000 PPS, 100 PPS, 10 PPS, 5 PPS, and 1 PPS. The frequency division is accomplished by eight decade counters connected in cascade.

B. Block Diagram Description (Figure 3.2)

The one-megacycle sine wave from the basic oscillator is applied to pin 18 of the tuned oscillator-pulse shaper (MC-30) card 1 which develops a one-megacycle rectangular 6-4 wave.

The rectangular 6-4 wave from pin 10 is applied to the Signal Distribution Unit and to pin 22 of the decade counter (BC-30) card 2,

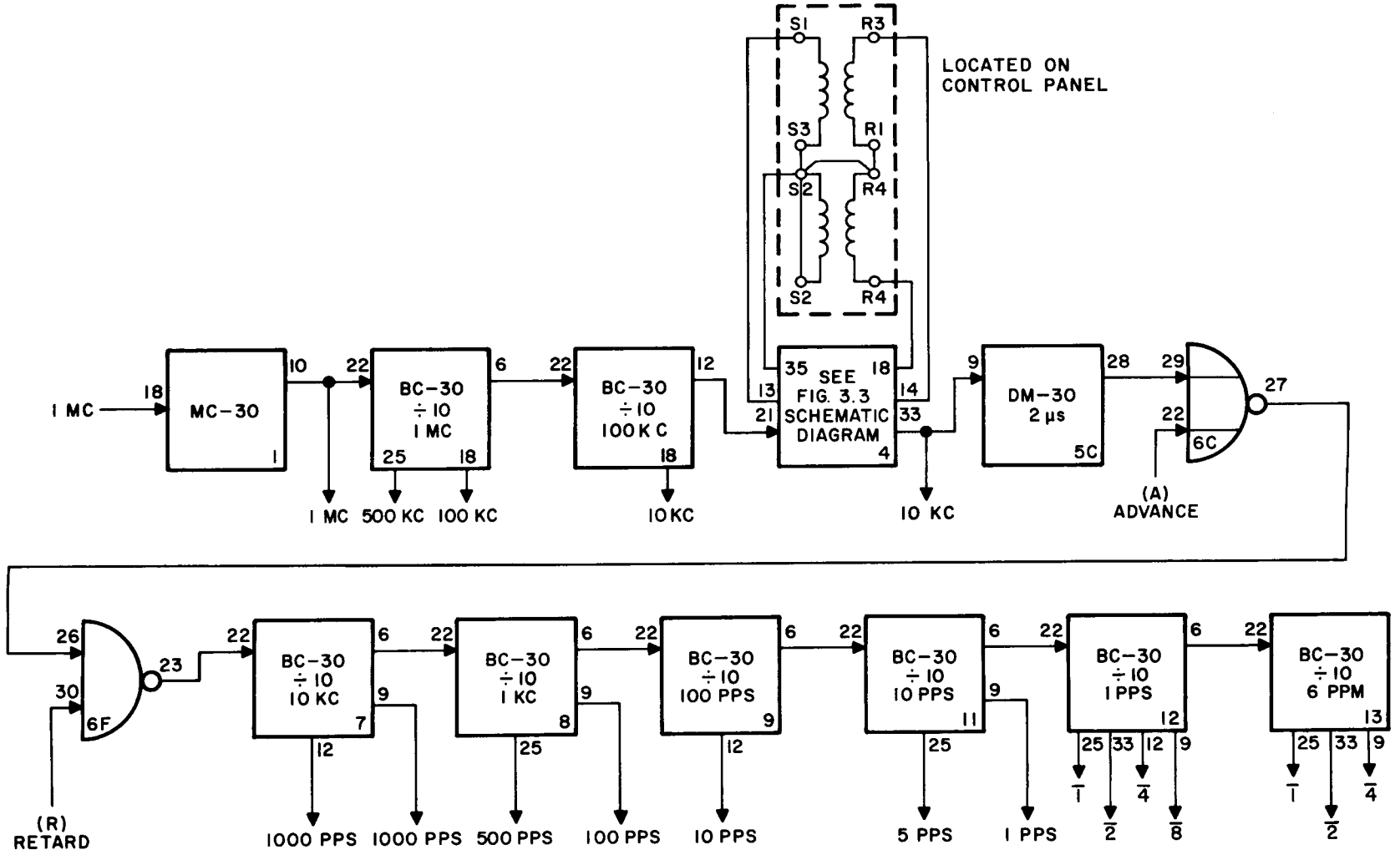


FIGURE 3.2 FREQUENCY DIVIDER, FUNCTIONAL BLOCK DIAGRAM

which provides both a 2:1 (500,000-PPS) and a 10:1 (100,000-PPS) output. The 500,000-PPS signal from pin 25 is coupled through a buffer inverter to the Signal Distribution Unit. The 100,000-PPS output from pin 18 is brought out through a buffer inverter for future use. The 100,000-PPS output from pin 6 is connected to pin 22 of the decade counter (BC-30) card 3 which provides a 10:1 (10,000-PPS) output. The 10,000-PPS output from pin 18 is brought out through a buffer inverter for future use. The 10,000-PPS output from pin 12 is connected to pin 21 of the phase shifter (SC-30A) card 4.

The input circuit of the phase shifter is a 10-KC tuned filter. The output from the tuned filter is a 10-KC sine-wave which is applied to the resolver which is used to advance or retard the timing signal. This feature allows the timing signal to be adjusted to coincide with WWV time interval signals. The controlled 10-KC signal is applied through emitter followers to a pulse shaper circuit to develop a 10,000-PPS square-wave output.

The 10,000 PPS is applied to pin 9 of the 2-microsecond Delay Multivibrator (DM-30), card 5. The output from pin 28 is a 2-microsecond-wide pulse with a repetition rate of 10,000 PPS.

The 2-microsecond pulse is applied to pin 29 of the "or" gate (DI-30) card 6C where it may be "ored) with a signal from the advance-retard circuit. The output from pin 27 is applied to pin 26 of the "and" gate (Di-30) card 6 where it may be "anded" with a signal from the advance-retard circuit.

The output from pin 23 of the "and" gate, which is normally 10,000 PPS, is applied to decade counter (BC-30), card 7. There are three 10:1 (1,000-PPS) outputs from this stage. Two of these outputs taken from pins 12 and 9 are connected through buffer inverters to the Binary Time Code Generator. The 1,000 PPS from pin 6 is utilized as one of the inputs to the advance-retard circuit and is also connected to pin 22 of the decade counter (BC-30) card 8, which provides both a 2:1 (500-PPS) and a 10:1 (100-PPS) output.

The 500-PPS output from pin 25 is utilized as one of the inputs to the Time Comparison Circuit. The 100-PPS output from pin 9 is applied through a buffer inverter to the Binary Time Code Generator. The 100-PPS output from pin 6 is utilized as one of the inputs to the advance-retard circuit and is also connected to pin 22 of the decade counter (BC-30) card 9, which provides a 10:1 (10-PPS) output.

The 10-PPS output from pin 12 is applied through a buffer inverter to the Digital Clock. The 10-PPS output from pin 6 is applied through two buffer inverters connected in cascade to the Binary Time Code Generator and as an input to the advance-retard circuit. The 10-PPS output from the first stage of the cascade buffer inverters is connected to the Digital Clock and to the Signal Distribution Unit. The 10 PPS is also connected to pin 22 of the decade counter (BC-30) card 11 which provides both a 2:1 (5-PPS) and a 10:1 (1-PPS) output.

The 5-PPS output from pin 25 is applied through a buffer inverter to the Binary Time Code Generator. The 1-PPS output from pin 9 is applied through a buffer inverter to the Digital Clock and to the Signal Distribution Unit and through another buffer inverter to the Binary Time Code Generator and as an input to the Time Comparison circuit. The 10-PPS output from pin 6 is connected to pin 22 of the decade counter (BC-30) card 12 which provides both a 2:1 and a 10:1 output.

The $\overline{1}$ output from pin 25 is connected through a buffer inverter to the Signal Distribution Unit. The 2-4-8 outputs from pins 33, 12, and 9 are connected through buffer inverters to the Signal Distribution Unit. The 8 output from pin 6 is connected to pin 22 of the decade counter (BC-30) card 13 which provides both a 2:1 and a 6:1 output.

The $\overline{1}$ output from pin 25 is connected through a buffer inverter to the Signal Distribution Unit. The $\overline{2}$ output from pin 33 and the $\overline{4}$ output from 9 are coupled through buffer inverters to the Signal Distribution Unit.

Provisions are made through the Reset Seconds Switch S1 to reset both card 12 and card 13 to the zero state.

3.3 CIRCUIT THEORY

A. General

The theory of operation of the special circuits contained in the Frequency Divider chassis is presented in the following paragraphs. Some of the circuits used are standard S-PAC Digital Modules and the theory of operation of these circuits can be found in paragraph 3.1 and in the manufacturer's instruction manual referenced in Table 1.1.

B. Phase-Shifter Circuit

(1) General

The Phase-Shifter circuit, Figure 3.3, is the fourth card of the Frequency Divider. This circuit is used in conjunction with the Time Comparison Circuit to obtain initial fine synchronization between the timing system and Radio Station WWV. This circuit is also used to maintain the fine synchronization on a daily and weekly basis.

(2) Circuit Description

The 10-KC rectangular 6-4 wave from pin 12 of the second divide-by-ten decade counter is applied to pin 21 through resistor R1 to the tuned circuit composed of inductor L1 and capacitors C1 and C2.

The 10-KC sine-wave output from the tuned circuit is coupled through capacitor C3 to the Darlington emitter-follower circuit composed of transistors Q1 and Q2. The Darlington circuit and feedback capacitor C4 are used to prevent loading of the tuned circuit.

The output from the emitter of transistor Q2 is coupled through capacitor C4 to the stator terminal S1 of the Reeves Resolver R-150.

The resolver is essentially a rotatable transformer consisting of a rotor and stator. The stator is the fixed primary and the rotor is composed of two secondary windings at right angles to each other, the angle of 90 degrees being maintained between them as they are rotated.

The rotation of the resolver is controlled by the "resolver dial" located on the control panel. The dial is calibrated to read the rotation of the resolver in microseconds with one complete rotation equal to 100 microseconds.

After an angular displacement, voltages of the same phase but of different amplitudes are induced in each of the rotor windings; the phase of the output can be changed continuously and without limit.

The output taken from terminal R3 of the rotor is coupled to the Darlington emitter-follower circuit composed of transistors Q3 and Q4. The output from the emitter of Q4 is coupled through variable resistor R11 and resistor R12 to the Darlington emitter-follower

circuit composed of transistors Q7 and Q8.

The output taken from the rotor terminal R2 is coupled to the Darlington emitter-follower circuit composed of transistor Q5 and Q6. The output from the emitter of Q6 is coupled through capacitor C6 to the Darlington emitter-follower circuit composed of transistors Q7 and Q8.

The variable resistor R11 is adjusted until its resistance equals the reactance of capacitor C6 at the operating frequency of 10 KC.

The output from the emitter of Q8 is coupled through capacitor C7 and resistor R15 to the base of transistor Q9.

Transistors Q9 and Q10 operate as overdriven amplifiers. The output from the collector of Q10 is a 10 KC-pulsed output clamped at ground and a negative ten volts.

C. Advance-Retard Circuit

(1) General

The Advance-Retard Circuit, Figure 3.4, is used in conjunction with the Time Comparison circuit to provide coarse synchronization of the Time Standard to Radio Station WWV.

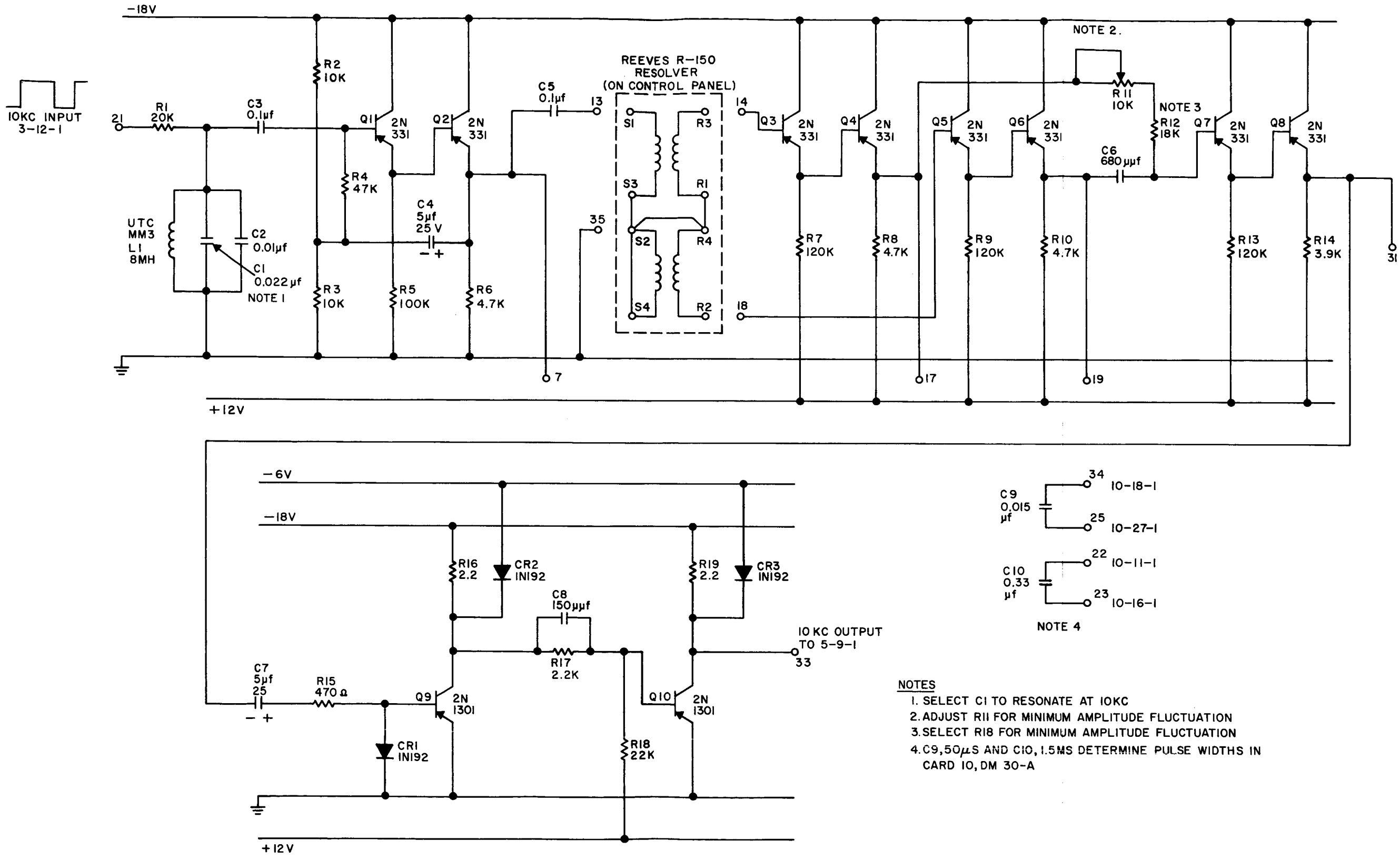
NOTE

This circuit should only be used during the initial synchronization procedure of the timing system to Radio Station WWV or resynchronization following a complete power failure.

(2) Circuit Description

The Advance-Retard Circuit utilizes S-PAC Digital Modules. The theory of operation of these circuits may be found in section 3.1 and in the manufacturer's instruction manual referenced in Table 1.1. The number of pulses added or deleted from the divider chain each second is determined by the setting of the Rate-Selector switch S1.

To result in a change of 1 millisecond per second of the locally generated timing signal, the Rate-Selector switch S1 is set to the 1MS/Sec position. This, in effect, feeds back the 10-PPS output from the divider chain.



NOTES

1. SELECT C1 TO RESONATE AT 10KC
2. ADJUST R11 FOR MINIMUM AMPLITUDE FLUCTUATION
3. SELECT R18 FOR MINIMUM AMPLITUDE FLUCTUATION
4. C9, 50μS AND C10, 1.5MS DETERMINE PULSE WIDTHS IN CARD 10, DM 30-A

FIGURE 3.3. PHASE-SHIFTER CIRCUIT

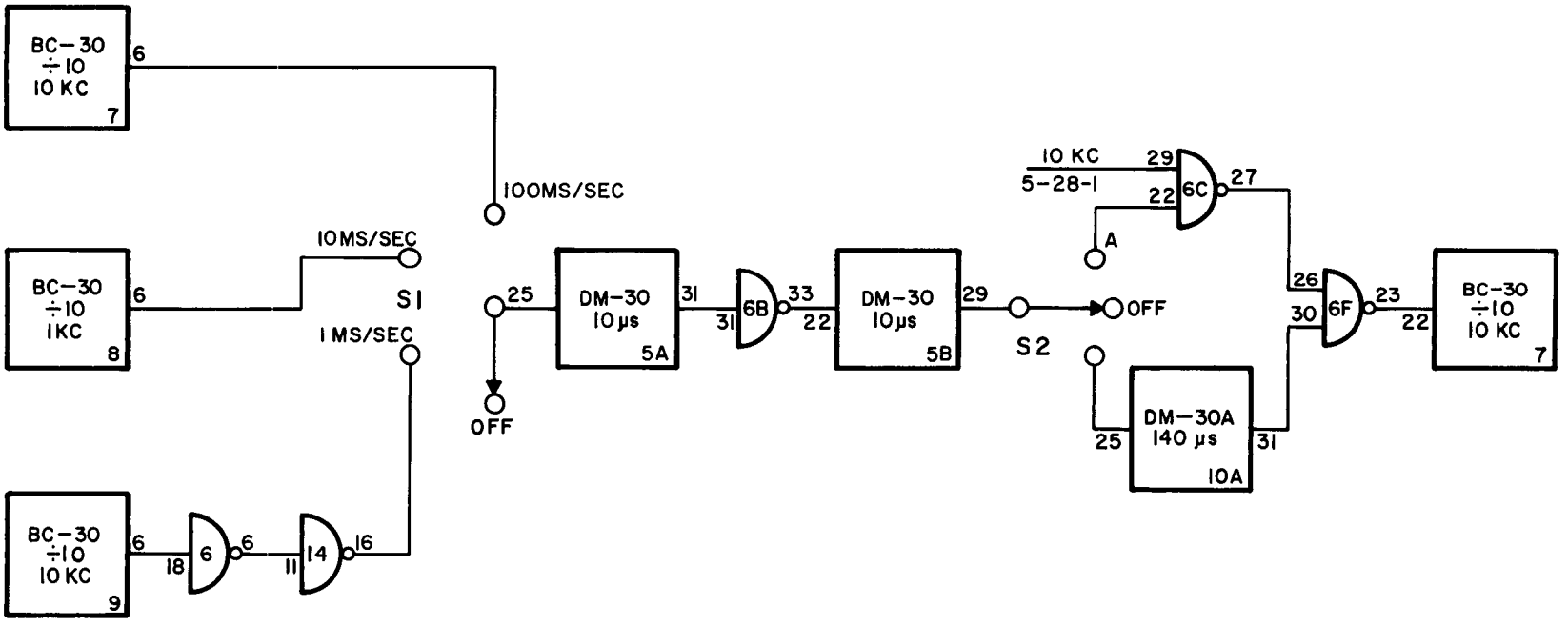


FIGURE 3.4 ADVANCE-RETARD CIRCUIT, FUNCTIONAL BLOCK DIAGRAM

To result in a change of 10 milliseconds per second of the locally generated timing signal, the Rate-Selector switch S1 is set to the 10-MS/Sec position. This, in effect, feeds back the 100-PPS output from the divider chain.

To result in a change of 100 milliseconds per second of the locally generated timing signal, the Rate-Selector switch S1 is set to the 100 MS/Sec position. This, in effect, feeds back the 1000-PPS output from the divider chain.

The Advance-Retard switch S2 is used to advance or retard the number of pulses generated by the divider chain in amounts determined by the Rate-Selector switch S1.

D. Time-Comparison Circuit

(1) General

The Time Comparison circuit, Figure 3.5, is used to mix the time interval signal from WWV with the 1-MS delayed marker 1-PPS signal from the Frequency Divider and to display this mixed signal on the Time Comparison oscilloscope.

(2) Circuit Description

The 1-PPS output from the Frequency Divider is applied to pin 22 of the adjustable Delay Multivibrator DM-30A. The output from pin 10 is a negative-going 1.5-millisecond pulse which is applied to pin 30 of the NAND Pac, Model DI-30, where it is gated with the negative-going 500-PPS signal from the Frequency Divider.

The output at pin 23 of the DI-30 is a one-millisecond-wide pulse with the positive edge occurring on the second. This is applied to the Time Comparison oscilloscope as an external trigger and to the Time Comparison circuit where it is mixed with the WWV time-interval signal.

The output from the Time Comparison circuit is the WWV time signal and the 1-MS delayed edge of the 1-PPS signal. When properly in sync with WWV, this positive pulse will occur at the positive zero crossing of the second cycle. This combined signal is applied to the vertical input of the Time Comparison oscilloscope.

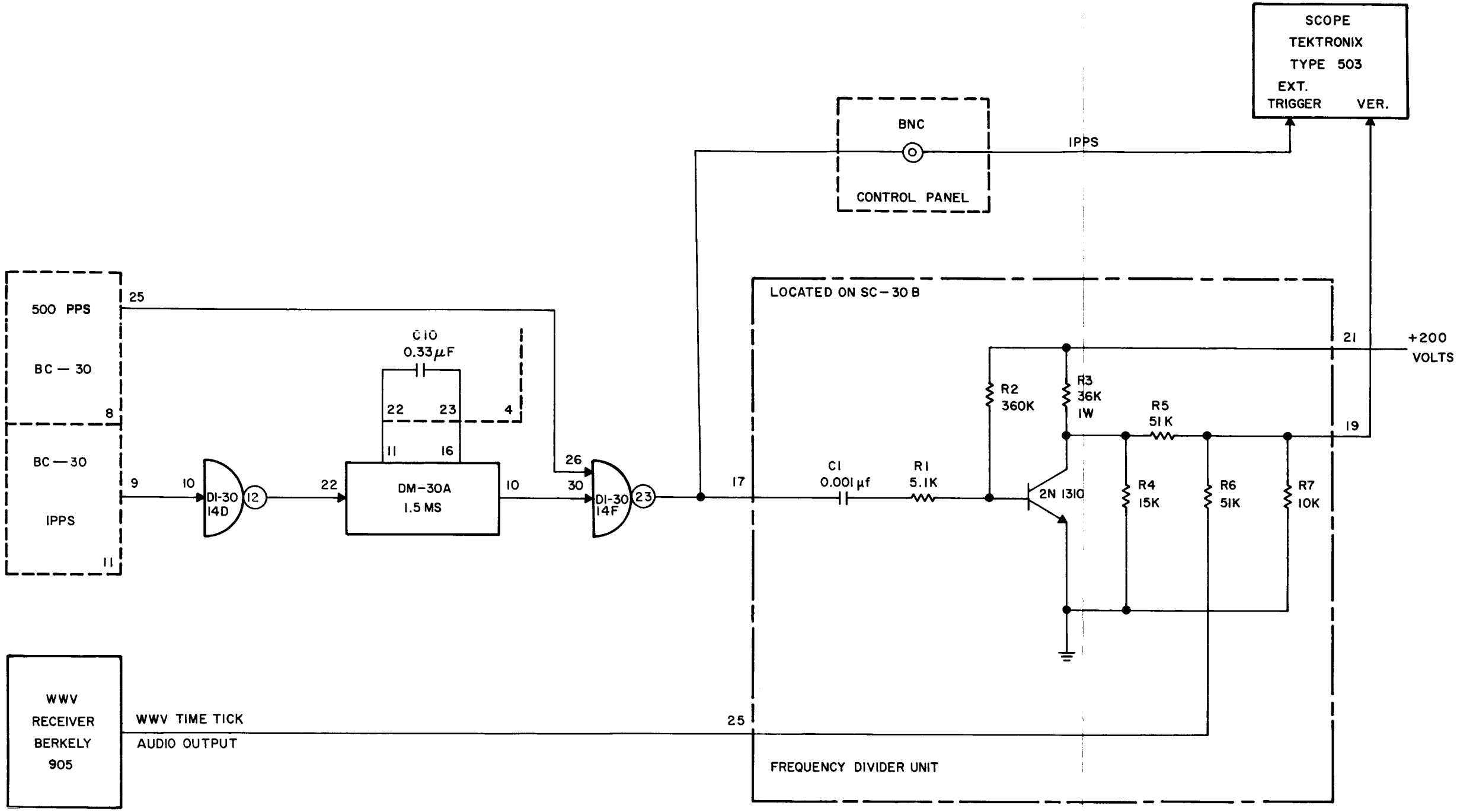


FIGURE 3.5. TIME COMPARISON CIRCUIT

E. 60-CPS Generator Circuit

(1) General

The 60-cps Generator Circuit, Figure 3.6, is used to develop a highly accurate and stable 60-cps sine wave which is used to operate the panel clock in synchronism with the 1-PPS signal developed by the frequency divider.

(2) Circuit Description

The 100-PPS output from the frequency divider chain is applied to the input (Pin 33) of the 600-cps synchronized oscillator circuit. Inductor L1, capacitors C4, C5, and C6 are tuned to resonate at 600 cps. The 600-cps output from the tuned circuit is coupled through capacitor C3 to the Darlington emitter-follower circuit composed of transistors Q4 and Q5. The Darlington circuit and feedback capacitor C7 are used to prevent loading of the tuned circuit. Variable resistor R18 is adjusted to provide a 4-volt PP signal.

The 600-cps output from pin 28 is applied to pin 9 of the Schmitt Trigger (ST-30). The output from pin 10 of the Schmitt Trigger is applied to pin 34 of the Decade Counter (BC-30). This decade is wired as a 5-4-2-1 counter and provides a square-wave output for shaping.

The output from pin 20 of the decade counter is a 60-PPS signal and is applied to pin 6 of the synchronized transformer driver located on card 16 (SC-30B).

The 60-cps output from pin 14 of the synchronizing transformer driver is applied to the synchronizing transformer. The output from the transformer is applied to the IT-226A ERA DC-AC inverter. The 105 VAC 60-cps output from the inverter is used to drive its numechron panel clock.

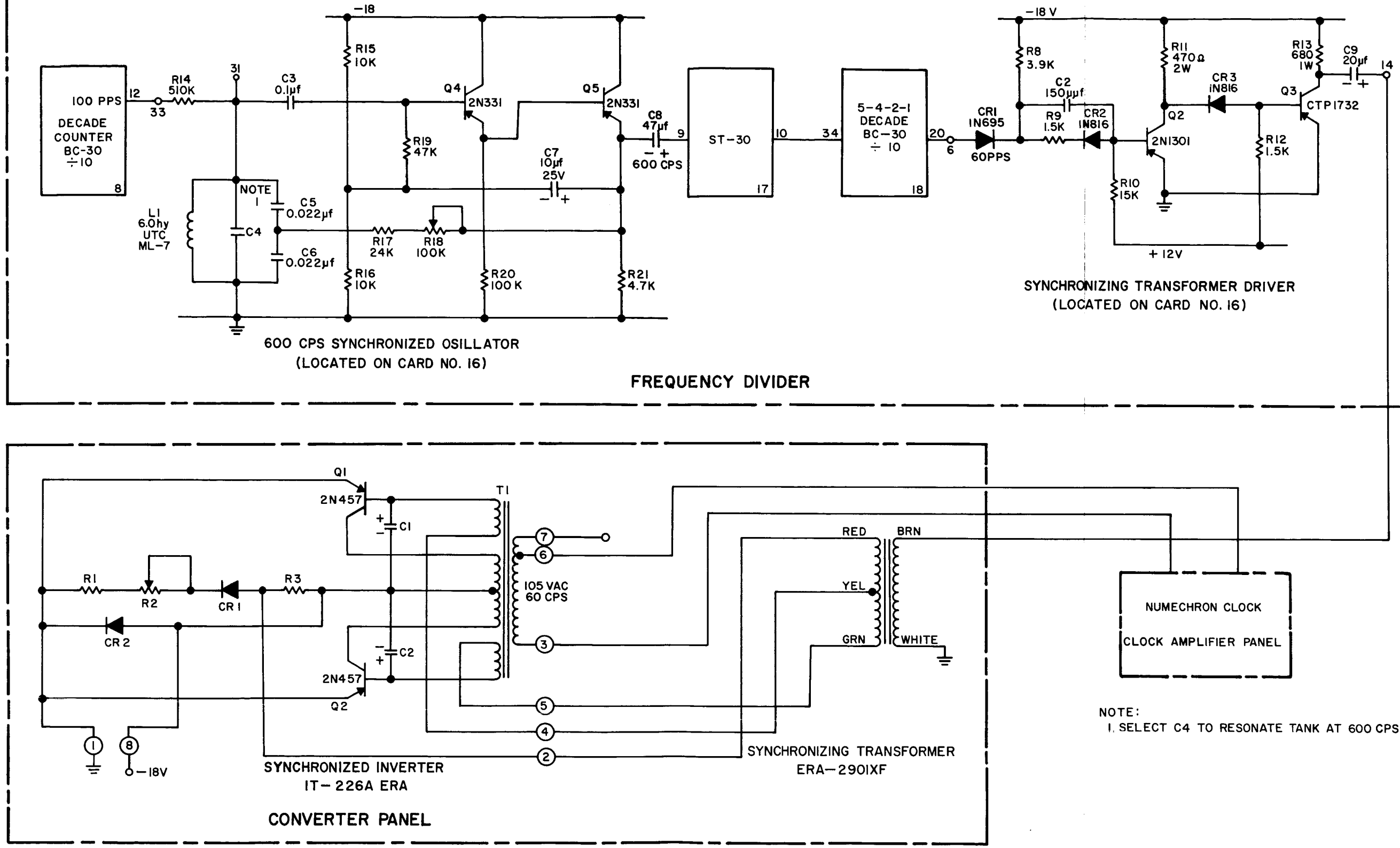


FIGURE 3.6.
60-CPS GENERATOR CIRCUIT AND SYNCHRONIZED INVERTER

3.4 DIGITAL CLOCK

A. General

The Digital Clock receives the highly stable and accurate 1-pulse-per-second signal from the frequency divider and, through appropriate decade counters connected in cascade, produces the 30-bit parallel binary-coded decimal time-of-the-year information.

The Digital Clock performs a series of scanning operations in order to convert the parallel binary-coded decimal time-of-the-day information into the serial decimal time-of-the-day information.

The 30-bit parallel binary-coded decimal time-of-the-year information is fed to the signal distribution unit where it is distributed to various digital displays and to the binary-time-code generator unit where it is converted to the NASA 1/sec BTC.

The serial decimal time-of-the-day information is fed to the distribution unit where it is distributed to various time-recording units.

One circuit in the digital clock produces a pulse every twenty-four hours to reset the units-of-hours and tens-of-hours counters to zero at the end of each twenty-four hour period.

Digiswitches are used to set the decade counters to a predetermined time when synchronizing the digital clock to Radio Station WWV.

B. Block-Diagram Description of the Digital Clock

For the following discussion refer to Figure 3.7 for the block diagram of the digital clock and to Figure 3.8 for the waveforms of the digital clock.

The 1-PPS signal from the frequency divider is applied to pin 9 of the delay multivibrator DM-30. The 10-microsecond-wide pulse from pin 17 of the DM-30 is applied to pin 6 of the NAND PAC DN-30 (card 4-A). With switch S7 in the "On" position the DN-30 serves as an amplifier inverter. The inverted 10-microsecond-wide pulse from pin 9 of the DN-30 is applied to pin 22 of the first decade counter.

Table 3.1 lists the functions performed by each of the decade counters.

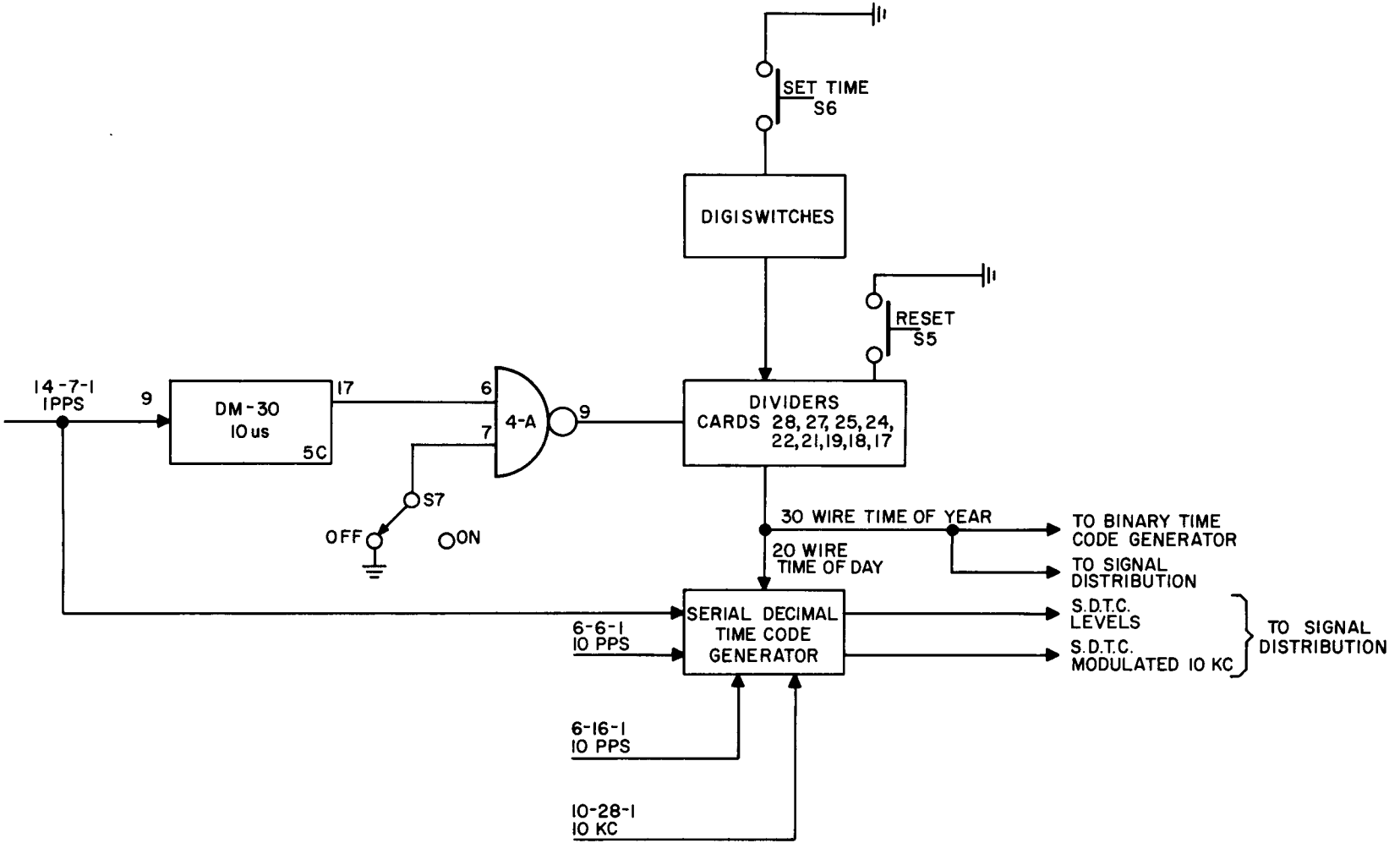


FIGURE 3.7
DIGITAL CLOCK, FUNCTIONAL BLOCK DIAGRAM

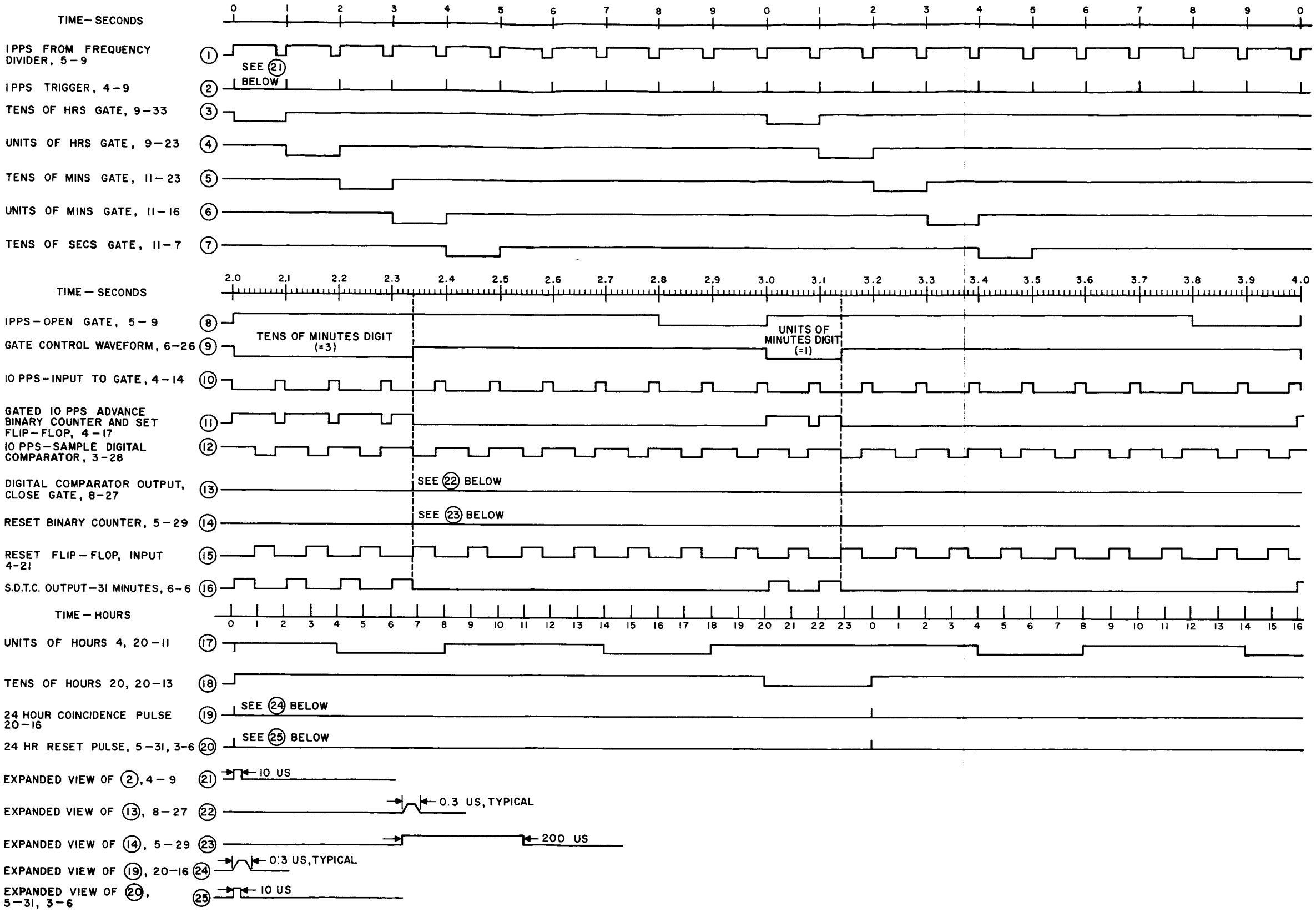


FIGURE 3.8. DIGITAL CLOCK, WAVEFORMS

TABLE 3.1 DIGITAL CLOCK COUNTER FUNCTIONS

Counter Stage No.	Input Signal	Division Factor	Output Signal	Bits of BCD Information
1	1 P/Sec.	10	6 PPM	4 - Units of Seconds
2	6 PPM	6	1 PPM	3 - Tens of Seconds
3	1 PPM	10	6 PPH	4 - Units of Minutes
4	6 PPH	6	1 PPH	3 - Tens of Minutes
5	1 PPH	10	1 P/10 Hrs.	4 - Units of Hours
6	1 P/10 Hrs.	2	1 P/Day	2 - Tens of Hours
7	1 P/Day	10	1 P/10 Days	4 - Units of Days
8	1 P/10 Days	10	1 P/100 Days	4 - Tens of Days
9	1 P/100 Days	4		2 - Hundreds of Days

From each decade counter an output is taken which represents 30-bit parallel binary-coded decimal time. Thirty signals, taken collectively, provide the information. Each signal is obtained from a decade counter stage and is a representation of the decade counters' count conditions.

Four circuits are required to provide ten digits for the units-of-seconds information and also for the units-of-hours information, units-of-days information, and tens-of-days information.

Three circuits are required to provide six digits for the tens-of-seconds information and also for the tens-of-minutes information.

Only two circuits are required to produce the tens-of-hours information since the only digits to be conveyed are a "0", "1" or a "2". Also, only two circuits are required to provide the hundreds-of-days information.

Each of the 30 signals is fed through a buffer inverter to the signal distribution unit.

At precisely 24:00:00 the tens-of-hours decade counter and the units-of-hours decade counter is reset to indicate "00". The 24-hour reset circuit used to accomplish this and the timing waveforms are shown in Figure 3.9.

With switch number 7 in the "Off" position the 1-pulse-per-second signal from the frequency divider is inhibited from being counted in the digital clock decade counters.

Depress the "Reset Switch" S5; this will reset all of the decade counters to the zero state. Set the days-of-the-year "Digiswitches" to the day of the year. Set the hours "Digiswitches" to the WWV voice announcement of the time of day. Set the minutes "Digiswitches" in advance of the announced time, and the seconds "Digiswitches" to zero.

Depress the "Time Set" switch, S5. The decade counters will be set to the information contained in the Digiswitches.

Listen to the received WWV time-interval signals. When the received time becomes equal to the time set in the digital clock, turn switch number 7 to the "On" position. This allows the 1 PPS to be counted by the decade counters.

Recheck the Digital Clock by listening to a voice announcement of the WWV time.

NOTE

WWV time signals are announced in Eastern Standard Time. When using these signals to set the digital clock, conversion to Greenwich mean time must be accomplished.

3.5 SERIAL DECIMAL TIME CODE GENERATOR

A. General

The Serial Decimal Time Code Generator receives the parallel binary-coded decimal time-of-day information from the Digital Clock and converts its to the Serial Decimal Time Code (SDTC).

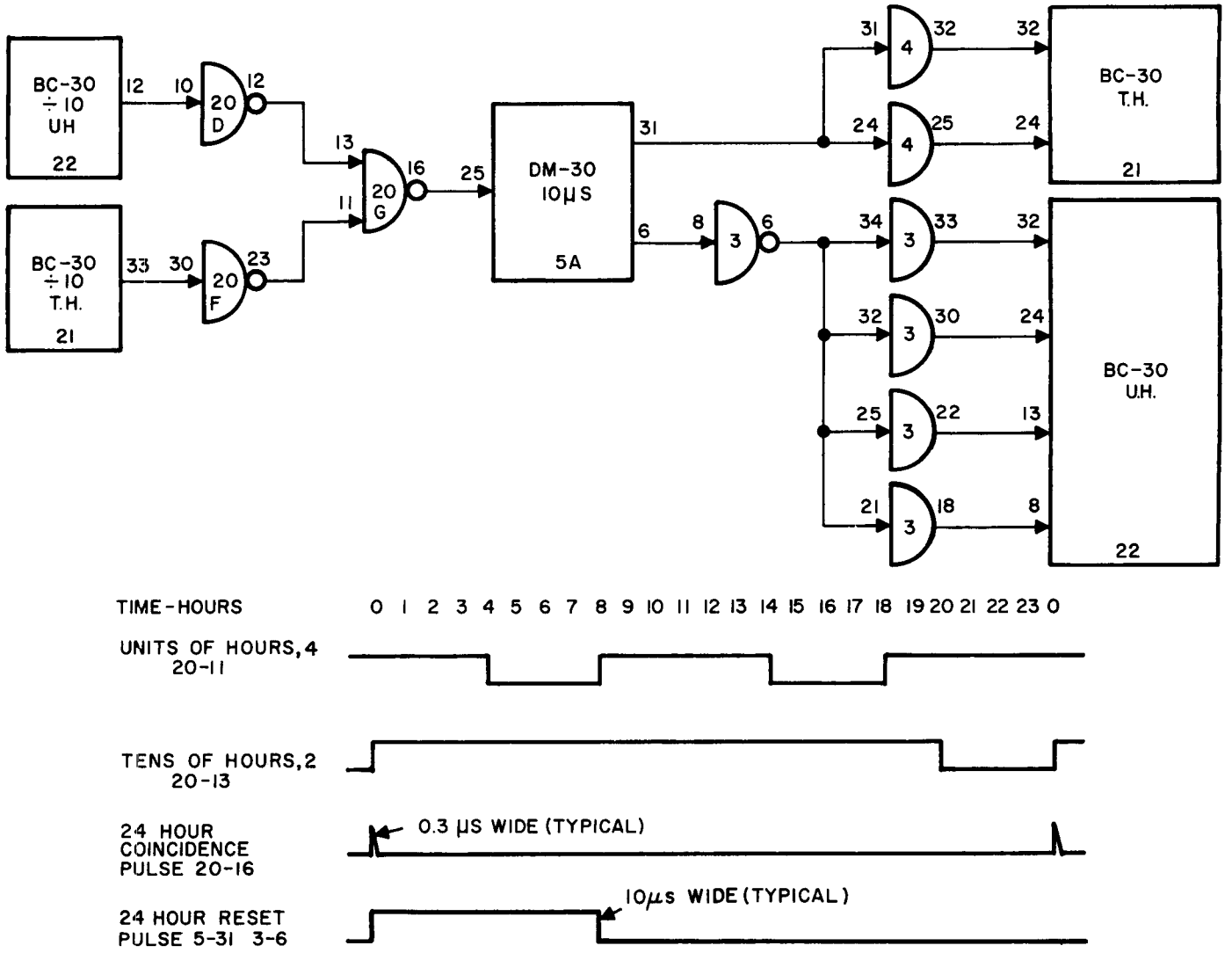


FIGURE 3.9 24-HOUR RESET CIRCUIT

B. Block Diagram Description (Figure 3.10)

The time information, in parallel, from the tens-of-hours, units-of-hours, tens-of-minutes, units-of-minutes, and tens-of-seconds decade counters in the Digital Clock is applied to the Scanner.

The tens-of-hours information passes through an Add One circuit before being applied to the Scanner. The purpose of the Add One circuit is to make the tens-of-hours time digit to appear larger by one than it actually is. That is, a zero will appear as one, a one will appear as two, etc.

Since the tens-of-hours digit is encoded at the start of a time frame, the Add One circuit will automatically cause the frame-marker pulse to appear in the time code.

The four outputs from the units-of-seconds decade counter are applied to the Binary-Coded Decimal-to-Decimal Decoder which produces five sequential timing pulses. These five pulses are applied to the scanner and determine which of the five time-of-day digits is to be scanned. For example, if the units-of-seconds counter is in the 0 (zero) state, the tens-of-hours digit (plus one) will appear at the output of the scanner. When the units-of-seconds counter is in the 1 (one) state, the units of hours will appear at the output of the scanner.

Table 3.2 shows the state of the units-of-seconds counter, the sequential timing pulse output from the BCD to Decimal Decoder, and the Time Digit at the output of the scanner.

TABLE 3.2. TIME DIGIT SCANNING SEQUENCE

State of Units of Seconds Counter	Output from BCD to Decimal Decoder	Time Digit at Output of Scanner
0	0	Tens of Hours (Plus one)
1	1	Units of Hours
2	2	Tens of Minutes
3	3	Units of Minutes
4	4	Tens of Seconds
5	-	---
6	-	---
7	-	---
8	-	---

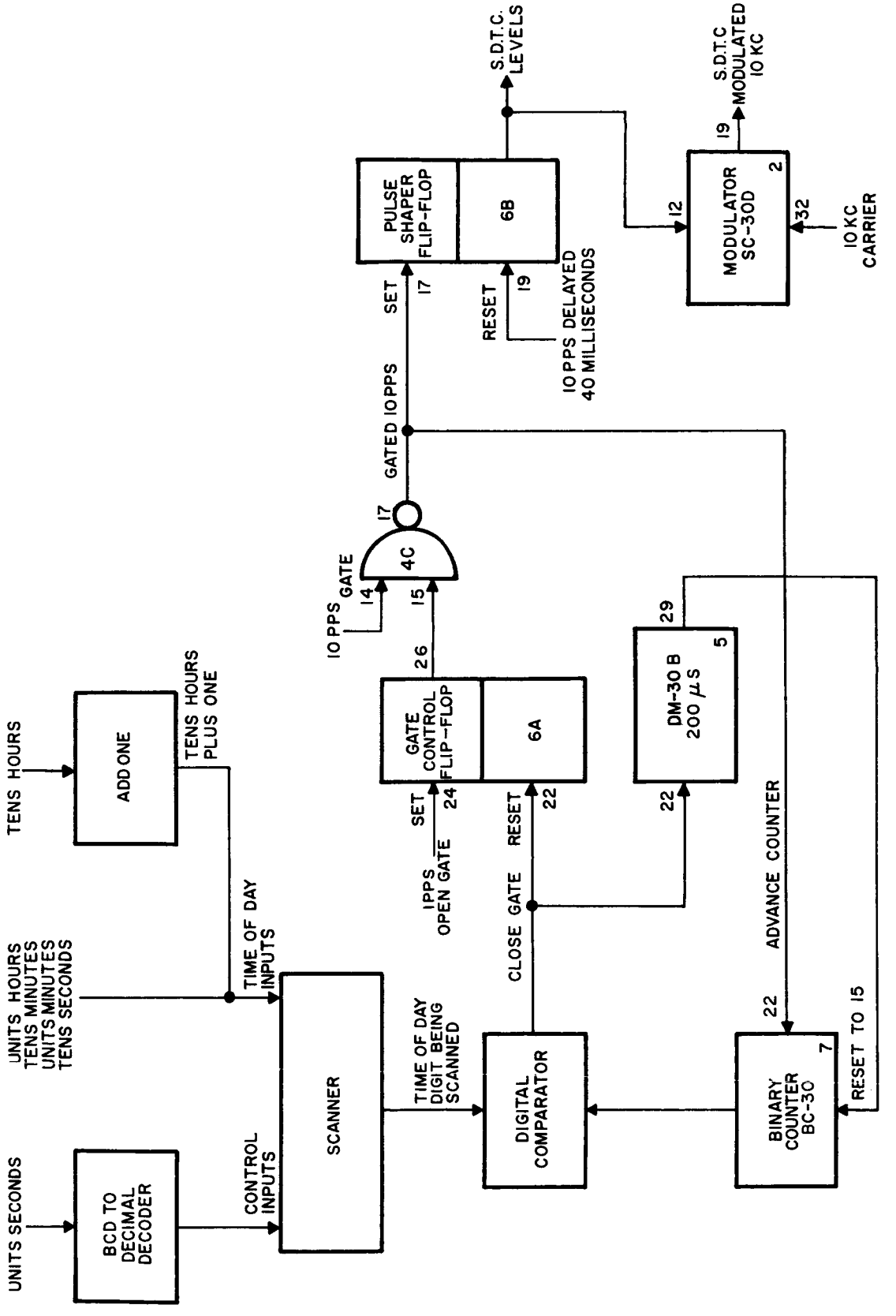


FIGURE 3.10 SERIAL DECIMAL TIME CODE GENERATOR
FUNCTIONAL BLOCK DIAGRAM

The 1 pulse-per-second signal from the Frequency Divider is used to set the gate control flip-flop, allowing the 10 pulse-per-second signal from the Frequency Divider to pass through the Gate.

The gated pulses are counted in the four-stage binary counter. The number stored in the binary counter is compared, in the Digital Comparator, with the time digit selected by the scanner to be encoded.

When the number in the binary counter becomes equal to the time digit being encoded, a positive transition occurs at the output of the Digital Comparator. This positive transition resets the gate control flip-flop causing the gate to inhibit the 10-pulse-per-second signal.

The positive transition from the Digital Comparator also triggers the reset pulse generator. The 200-microsecond-wide output pulse from the reset pulse generator resets the binary counter to the 15th state; this allowes the number of pulses passing through the gate to be one more than the time digit being encoded. This is in accordance with the Serial Decimal Time Code format.

The gated 10-pulse-per-second signal sets the Pulse Shaper flip-flop. The purpose of this flip-flop is to standardize the Serial Decimal Time Code pulse widths. The Pulse Shaper flip-flop is reset 40 milliseconds after it was set by a 10-pulse-per-second signal from the Frequency Divider.

The output of the Pulse Shaper flip-flop is the Serial Decimal Time Code which is coupled to the Signal Distribution Unit and to the Modulator where it is used to modulate a 10-KC carrier frequency. This modulated output is coupled to the Signal Distribution Unit.

3.6 CIRCUIT THEORY

A. General

The theory of operation of the special circuit contained in the Digital Clock chassis is presented in the following paragraph. All other circuits used are standard S-PAC Digital Modules and the theory of operation of these circuits is contained in Section 3.1 and the manufacturer's instruction manual referenced in Table 1.1.

B. Modulator Circuit

1. General

The Modulator Circuit, Figure 3. 11, amplitude-modulates a 10-KC carrier in accordance with the dc-level changes of the serial decimal time code (SDTC).

2. Circuit Description

The 10-KC rectangular wave from the frequency divider is applied to the carrier input Pin 32 through resistor R1 and variable resistor R2 to the tuned circuit composed of inductor L1 and capacitors C1 and C2.

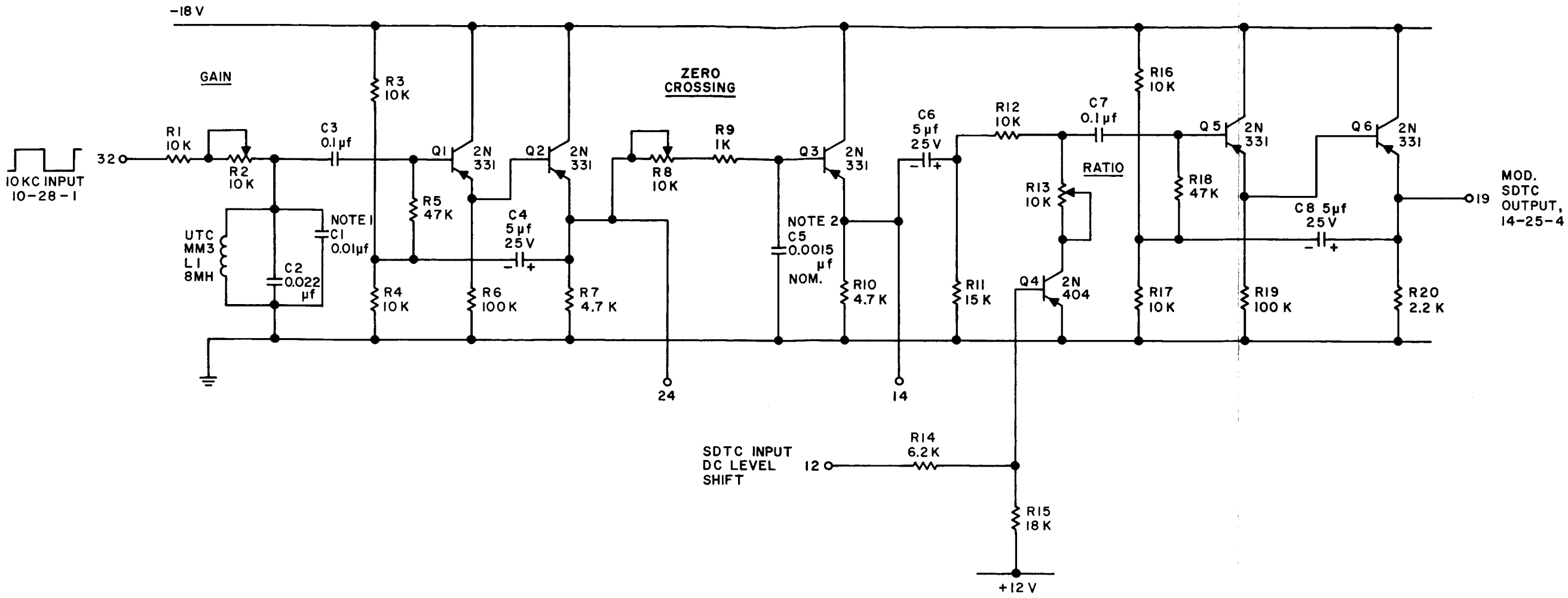
The 10-KC sine wave output from the tuned circuit is coupled through capacitor C3 to the Darlington Emitter-Follower Circuit composed of transistors Q1 and Q2. The Darlington emitter-follower circuit and feedback capacitor C4 prevent the tuned circuit from being overloaded.

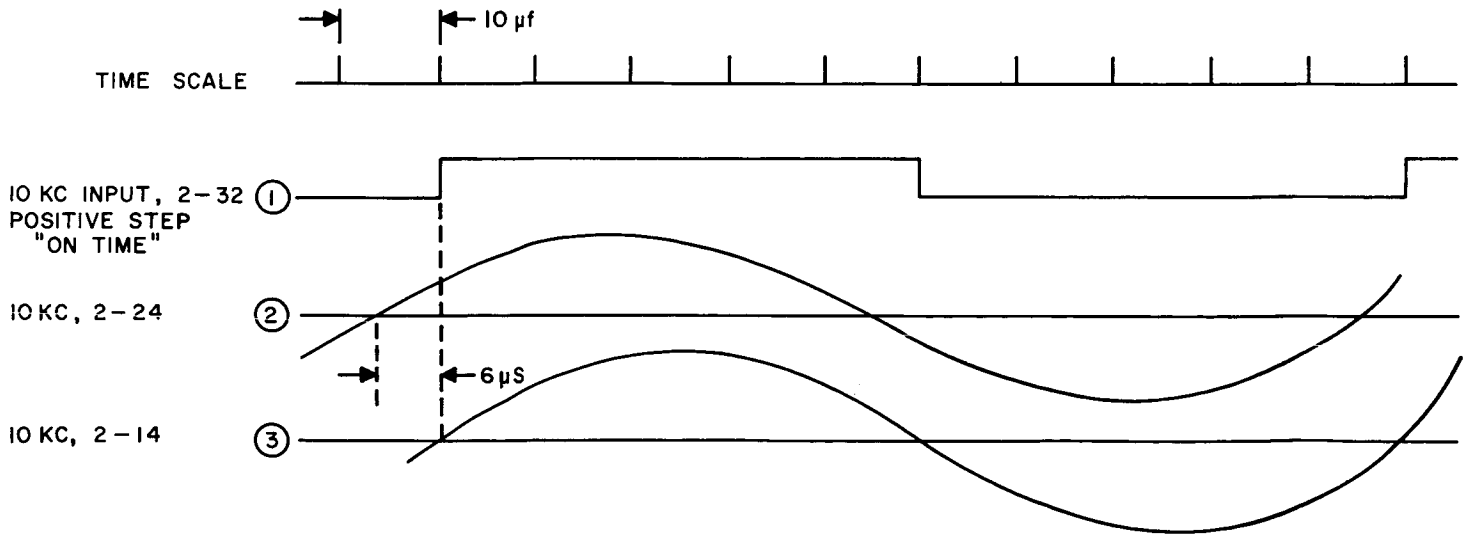
The output from the emitter of Q2 is applied to the phase lag network composed of variable resistor R8, resistor R9, and capacitor C5 which allows the zero crossings of the 10-KC carrier to occur in coincidence with the level changes of the serial decimal time code. The output from the lag network is buffered by emitter-follower transistor Q3.

The coupling network composed of capacitor C6 and resistor R11 removes the dc level from the 10-KC carrier.

Resistor R12, variable resistor R13, transistor Q4, resistor R14, and resistor R15 compose an impedance modulator. When the serial decimal time code input at Pin 12 is at the zero-volt level, transistor Q4 is cut off allowing the 10-KC carrier to pass through the circuit unattenuated. When the serial decimal time code is at the negative-six-volt (-6) level, transistor Q4 is saturated and the 10-KC carrier is attenuated by the voltage-divider network composed of resistor R12 and variable resistor R13. Variable resistor R13 allows the ratio of the two carrier levels to be continuously varied.

The modulated carrier is coupled through capacitor C7 to the Darlington emitter follower composed of transistors Q5 and Q6.





NOTES

1. RESONATE AT 10KC, NOMINAL (DETUNE UNTIL POSITIVE GOING ZERO CROSSING OF 10KC AT PIN 24 LEADS "ON TIME," POSITIVE STEP AT PIN 32, BY APPROXIMATELY 6 µS)
2. SELECT C5 TO ALLOW APPROXIMATELY EQUAL PHASE SHIFT EACH SIDE OF ON TIME MARK (POSITIVE STEP, PIN 32) WHEN R8 IS VARIED FROM MINIMUM TO MAXIMUM.

FIGURE 3.11. MODULATOR CIRCUIT FOR SERIAL DECIMAL TIME GENERATOR

The Modulated serial decimal time code output is taken from the emitter of transistor Q6 (Pin 19).

3.7 SERIAL DECIMAL TIME CODE

A. Format Description

The following description is given in conjunction with Figure 3.12. As the name "serial decimal time code" implies, the number of pulses used to encode a time digit is equal to the value of the digit being encoded. For example, to encode the digit four would require four pulses and to encode the digit five would require five pulses.

The following points are of importance in understanding the serial decimal time code:

1. The start of a time digit is marked by an extra pulse.
2. The start of a time frame is marked by an extra pulse.
3. The time encoded is the time at the start of the frame.
4. Frame rate - one frame per ten seconds.
5. Digit rate - one digit per second.
6. Pulse rate - ten pulses per second.
7. Time digits encoded - tens and units of hours, tens and units of minutes, and tens of seconds.
8. The most significant time digits are encoded first: tens of hours, units of hours, tens of minutes, etc.

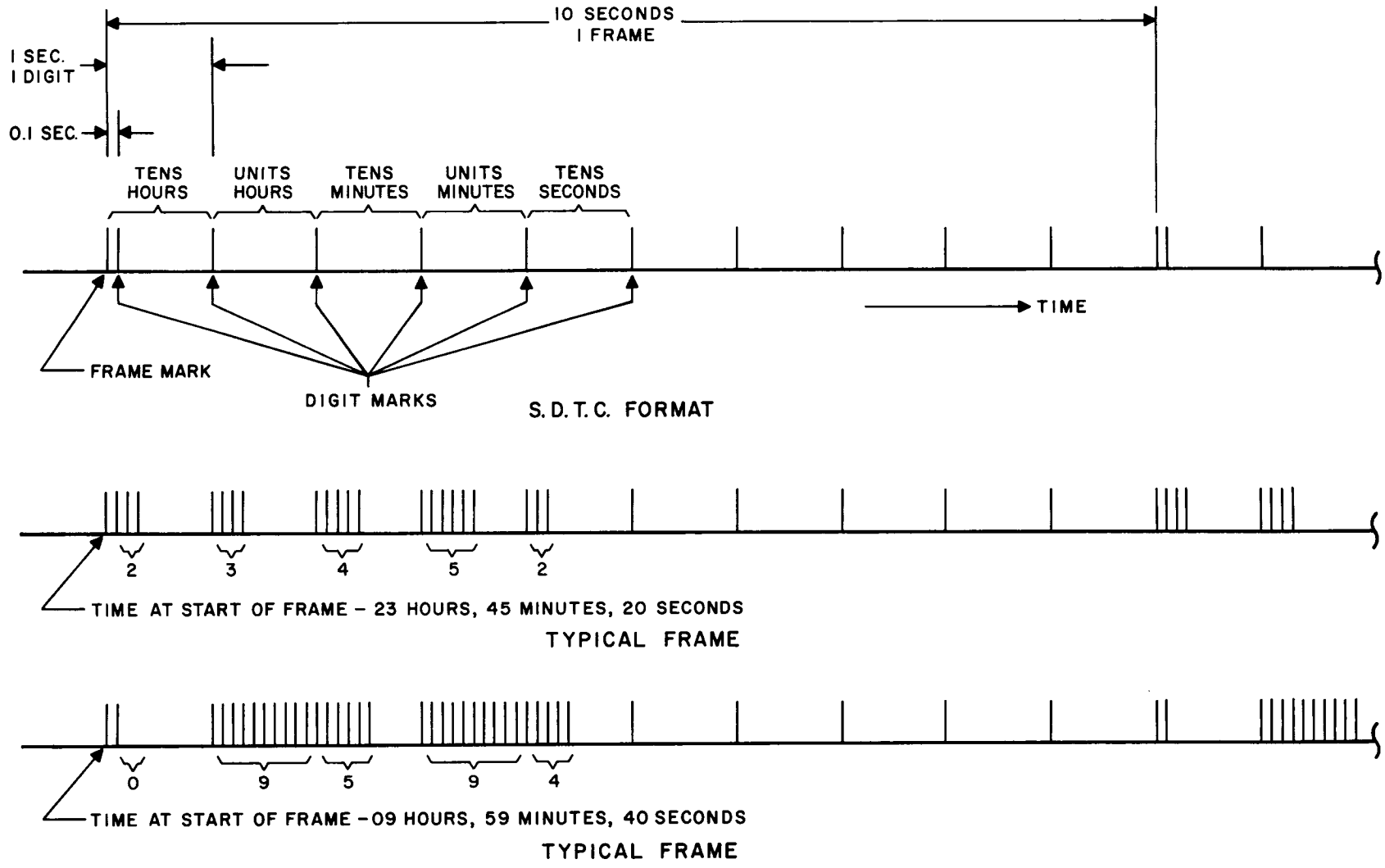


FIGURE 3.12 SERIAL DECIMAL TIME CODE FORMAT

B. Checking the Serial Decimal Time Code Generator

Should it ever become necessary to check the operations of the serial decimal time code generator, the following procedure is recommended:

1. Turn the "ON-OFF" switch of the digital clock located on the control panel to the "OFF" position. This will prevent the 1-pulse-per-second signal from the frequency divider from advancing the digital clock.

2. Depress the "RESET" switch. This will reset the digital clock decade counters to the "ZERO" (0) state.

3. Set the units-of-seconds digiswitch to 0, 1, 2, 3, or 4, depending on the time-of-day digit to be checked. (See Table 3.2.)

4. After the time-of-day digit has been selected, dial in all possible digits on the corresponding digiswitch.

5. Depress the "SET" switch. This will set into the binary counter the number selected by the digiswitch. Reset the digital clock before inserting the next number.

6. Observe the serial decimal time code pattern on an oscilloscope. The number of pulses appearing in the time code frame should be one more than the number dialed into the corresponding digiswitch.

NOTE:
When the tens-of-hours time digit is being checked the number of pulses appearing in the time frame will be two more than the number displayed on the tens-of-hours digiswitch.

3.8 BINARY TIME CODE GENERATOR

A. General

The Binary Time Code Generator receives the binary-coded decimal time-of-the-year information from the Digital Clock in parallel and converts it to the NASA 1/sec BTC. The code format, Figure 3.21, should be studied carefully before trying to understand the circuits used to produce the code.

B. Block Diagram Description

For the following discussion refer to Figure 3.13 for the block diagram, Binary Time Code Generator, and to Figure 3.14 for the waveforms, Binary Time Code Generator.

The information input to the Binary Time Code Generator consists of 30 wires containing time-of-year information, in parallel, from the Digital Clock and 4 wires which may be used in the future for station data.

The time information from any particular decade counter usually consists of four wires; however, the tens-of-seconds and the tens-of-minutes decade counters require only three wires to code their outputs while the tens-of-hours and hundreds-of-days decade counters require only two wires to code their outputs. The four wires from a decade counter are coded in the 1-2-4-8 code. The four wires are weighted, and the sum of the weight is equal to the decimal digit stored in the decade counter.

The 30-wire time-of-year information from the Digital Clock is fed into 30 identical 2-input "And" gates. The 30-wire inputs to the gates are completely in parallel form; that is, the individual decimal digits are in parallel and the bits that comprise each decimal digit are also in parallel.

At the beginning of each second the reset and read-in Pulse Generator produces a 200-microsecond-wide pulse that resets (clears) the 40-stage Shift Register. This pulse is followed by a delayed 200-microsecond-wide pulse that enables the 30, 2-input, "And" gates allowing the time-of-year information to be set into the 40-stage Shift Register. The unused input to the ten extra shift-register stages contains zeros.

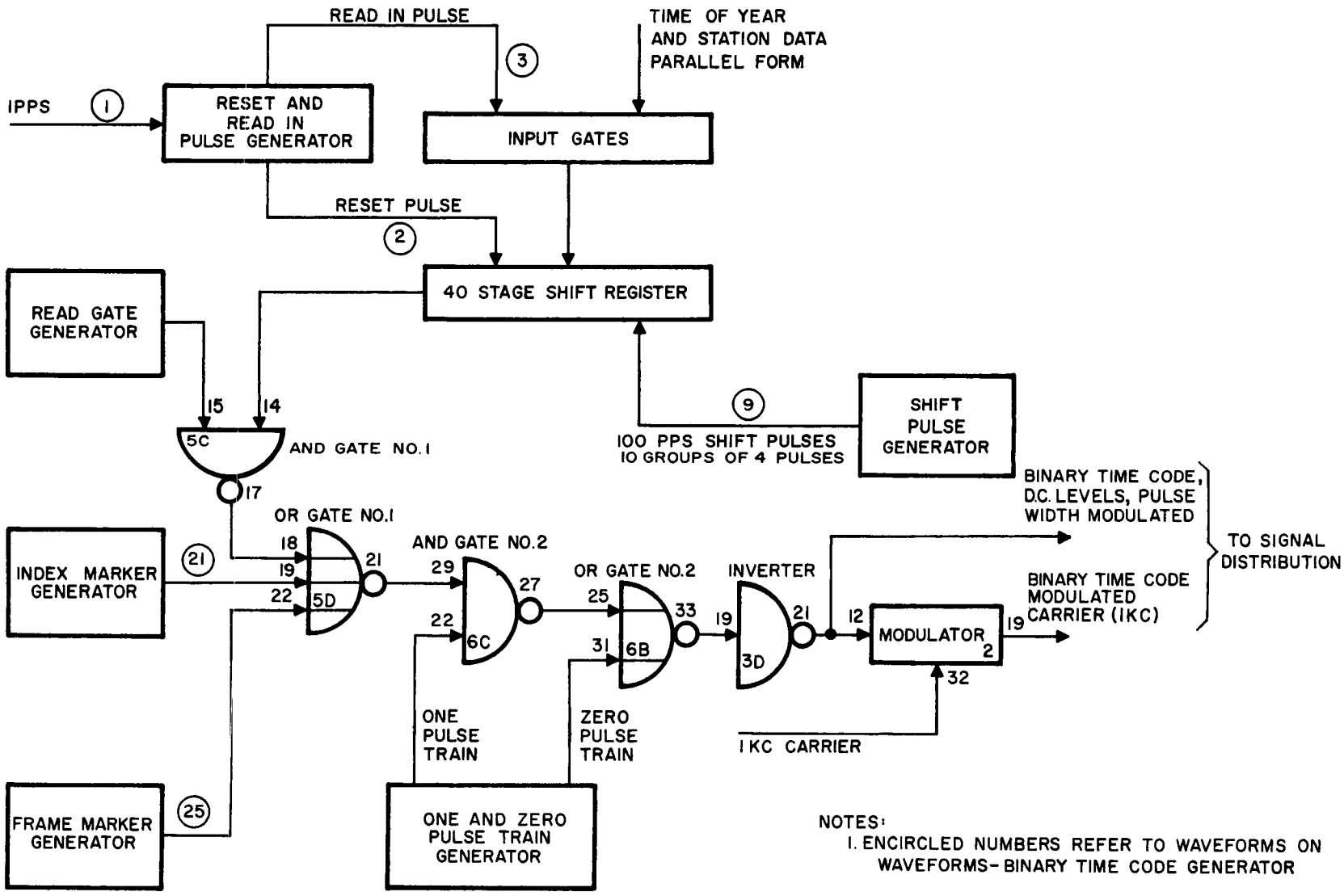


FIGURE 3.13 BINARY TIME CODE GENERATOR, FUNCTIONAL BLOCK DIAGRAM

Essentially, the 40-stage Shift Register, which is controlled by the Shift Pulse Generator, converts the digit parallel, bit parallel, time information to a digit serial, bit serial, one-wire output.

The Shift Pulse Generator produces 40 Shift Pulses per second, at a 100-pulse-per-second rate. These pulses are produced in 10 groups, each group containing 4 shift pulses.

The Frame Reference Marker generator generates a 50-millisecond-wide pulse that is at the binary "One" (negative six volts) only during the last five bit times of the time frame.

The Read Gate Generator generates ten 40-millisecond-wide pulses that enable the read gate, allowing the time information from the 40-stage shift register to be inserted into the time frame.

The Index Marker Generator generates nine 10-millisecond-wide pulses that are at the binary "One" (negative six volts) every 100 milliseconds from 100 milliseconds to 900 milliseconds.

It is now necessary to convert the time code from a dc-level shift to a pulse-width change, that is, to provide a wide pulse (6 milliseconds) when the time code is at the binary "One" level, in this case a negative 6 volts, and a narrow pulse (2 milliseconds) when the time code is at the binary "Zero", in this case zero volt. These requirements are met with the One and Zero pulse train generator.

The one-pulse-train output from the one- and zero-pulse-train generator is a 6-millisecond-wide pulse at a frequency of 100 pulses per second (bit rate) which is applied to Pin 22 of "And" gate number 2. The zero-pulse-train output is a 2-millisecond-wide pulse also at a frequency of 100 pulses per second (bit rate) which is applied to Pin 31 of "Or" gate number 2.

The dc-level shift time code is applied to "Or" gate number 1. When the output from this "Or" gate is at the binary "One" level (negative six volts) "And" gate number 2 is enabled, allowing the 6-millisecond-wide pulses to pass through the "And" gate and through "Or" gate number 2. When the output from the "Or" gate number 1 is at the binary "Zero" level (zero volt) "And" gate number 2 is inhibited and the 2-millisecond-wide pulse is allowed to pass through "Or" gate number 2. Thus, the dc-level shift time code has been converted to a pulse-width code.

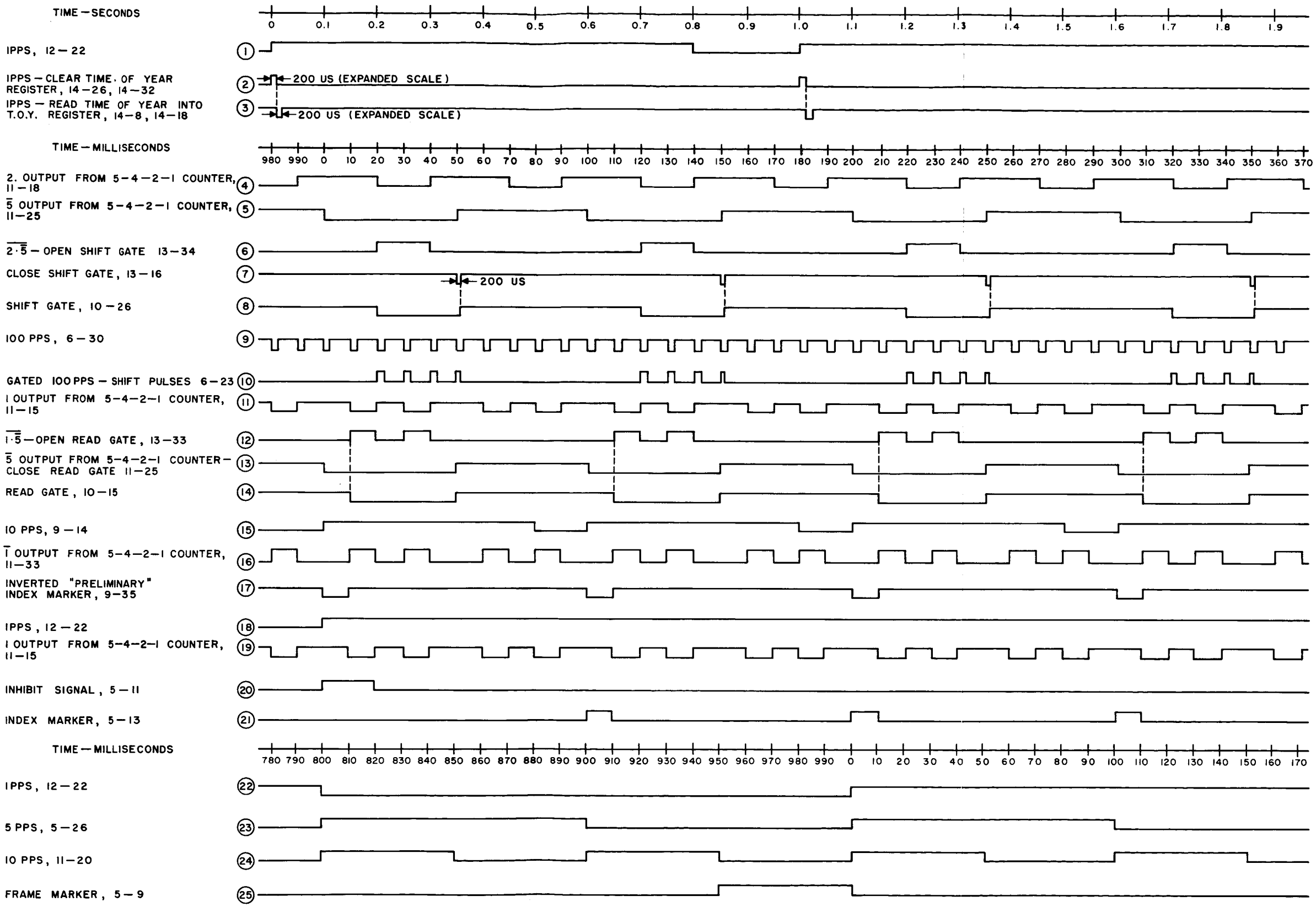


FIGURE 3. 14 WAVEFORMS, BINARY TIME CODE GENERATOR

3.9 CIRCUIT THEORY

A. General

The theory of operation of the special circuits contained in the Binary Time Code Generator is presented in the following paragraphs. All of the circuits, except the Modulator circuit, are standard S-PAC Digital Modules and the theory of operation of these circuits may be found in Section 3.1 and in the manufacturer's instruction manual referenced in Table 1-1.

B. Clear and Read-In Pulse Generator

1. General

The Clear and Read-In Pulse Generator, Figure 3.15, is used to produce, at the start of each second, a 200-microsecond-wide pulse that resets (clears) the 40-stage Shift Register. This pulse is followed by a delayed 200-microsecond-wide pulse that enables the Read Gate allowing the Time-of-Year information to be read into the 40-Stage Shift Register.

2. Circuit Description

The 1-pulse-per-second signal from the Frequency Divider is applied to Pin 22 of the delay multivibrator number 1. The output at Pin 29, which is a 200-microsecond-wide pulse, is applied to Pin 30 of inverter number 1 and to Pin 29 of inverter number 2.

The output from Pin 23 of inverter number 1 is applied to Pin 22 of power amplifier number 1 and to Pin 20 of power amplifier number 2.

The output from Pins 32 and 35 of power amplifier number 1 and from Pins 26 and 30 of power amplifier number 2 is a positive-going 200-microsecond-wide pulse that clears (resets) the 40-Stage Shift Register at the beginning of each second.

The output from Pin 27 of inverter number 2 is applied to Pin 25 of delay multivibrator number 2. The output at Pin 6, which is a delayed 200-microsecond-wide pulse, is applied to Pin 9 of inverter number 3.

The output from Pin 7 of inverter number 3 is applied to Pin 10

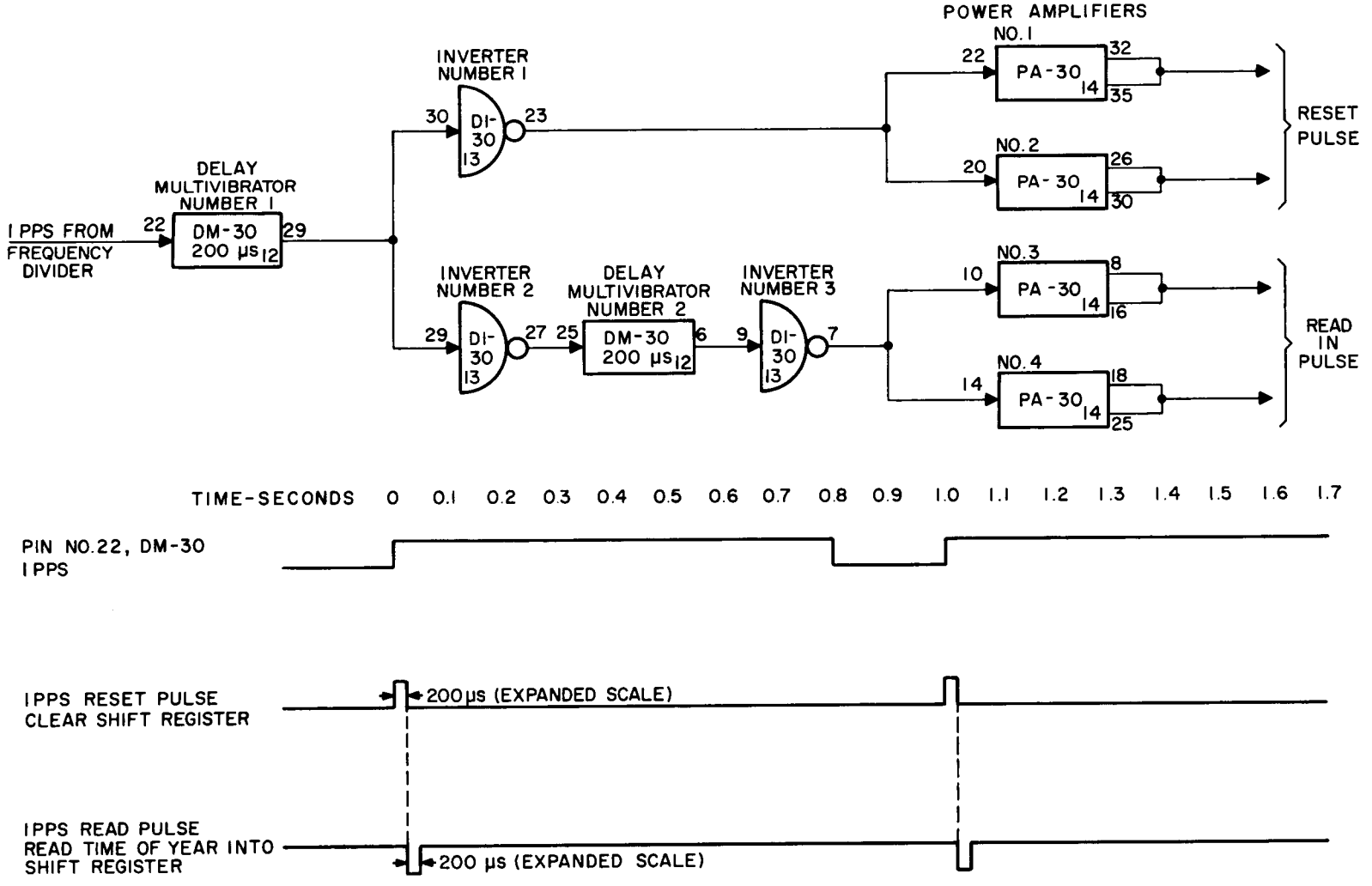


FIGURE 3.15 CLEAR AND READ-IN PULSE GENERATOR

of power amplifier number 3 and to Pin 14 of power amplifier number 4.

The output from Pins 8 and 16 of power amplifier number 3 and from Pins 18 and 25 of power amplifier number 4 is a negative-going 200-microsecond-wide pulse that enables the Read Gates, allowing the time-of-year information to be read into the 40-stage Shift Register.

C. Frame Marker Generator

1. General

The Frame Marker Generator, Figure 3.16, generates a 50-millisecond-wide pulse once each second during the last five bit times of the time frame to mark the beginning of the one-second time frame.

2. Circuit Description

The 1-pulse-per-second and the 5-pulse-per-second signals from the Frequency Divider are applied to the "And" gate at Pins 6 and 26, respectively. The 10-pulse-per-second signal from Pin 20 of the 5-4-2-1 decade counter is applied to Pin 7 of the "And" gate.

When the three inputs to the "And" gate are at the binary "One" (negative six volts), a positive transition will occur at Pin 9 of the "And" gate.

As shown by the timing waveforms at the bottom of Figure 3.16, this positive transition, which is a 50-millisecond-wide pulse, will occur, once each second, at 950 milliseconds to mark the beginning of the time frame.

D. Shift Pulse Generator

1. General

The Shift Pulse Generator, Figure 3.17, produces 40 shift pulses per second, at a 100-pulse-per-second rate. These pulses are produced in 10 groups with each group containing 4 shift pulses.

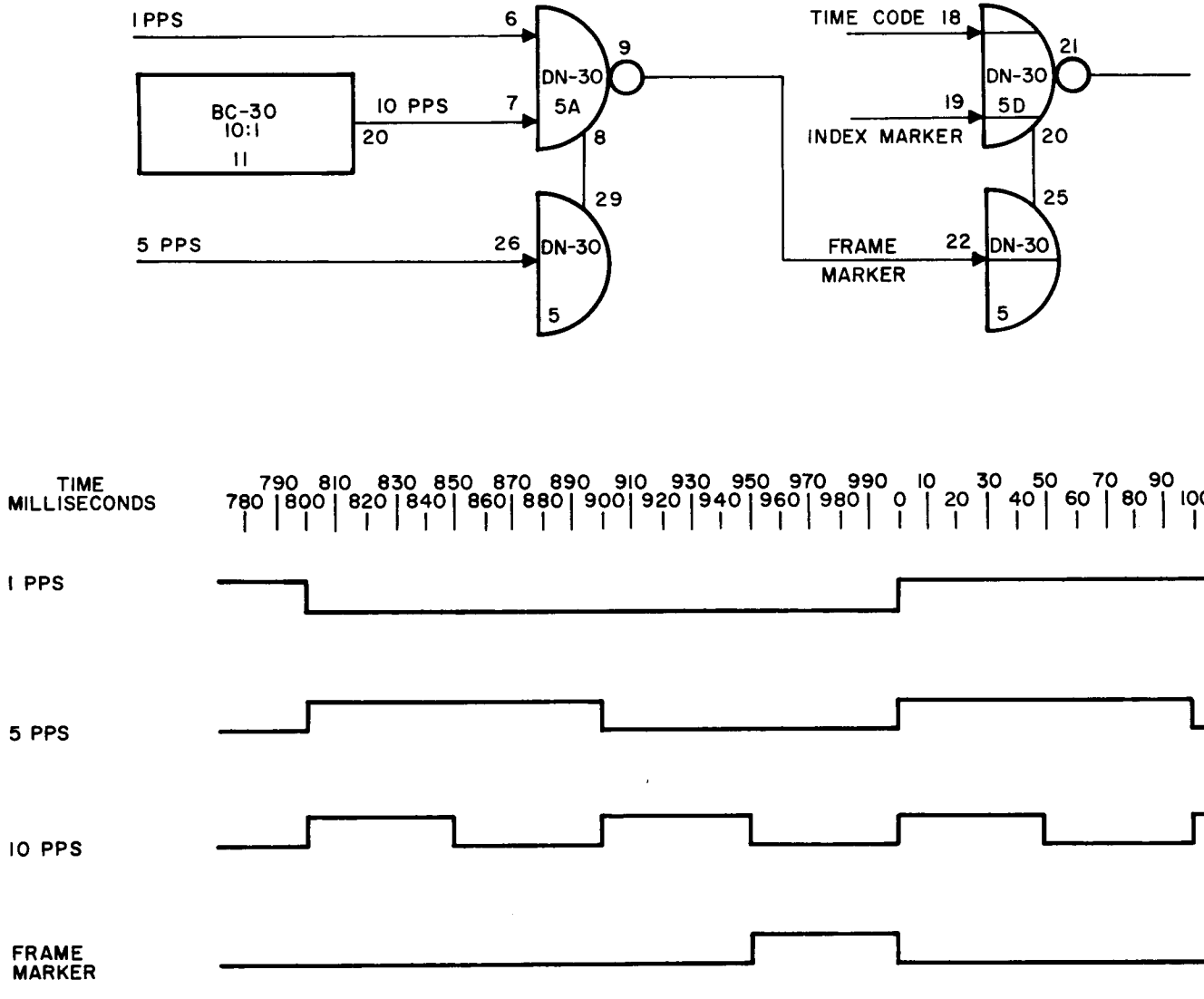


FIGURE 3.16 FRAME MARKER GENERATOR

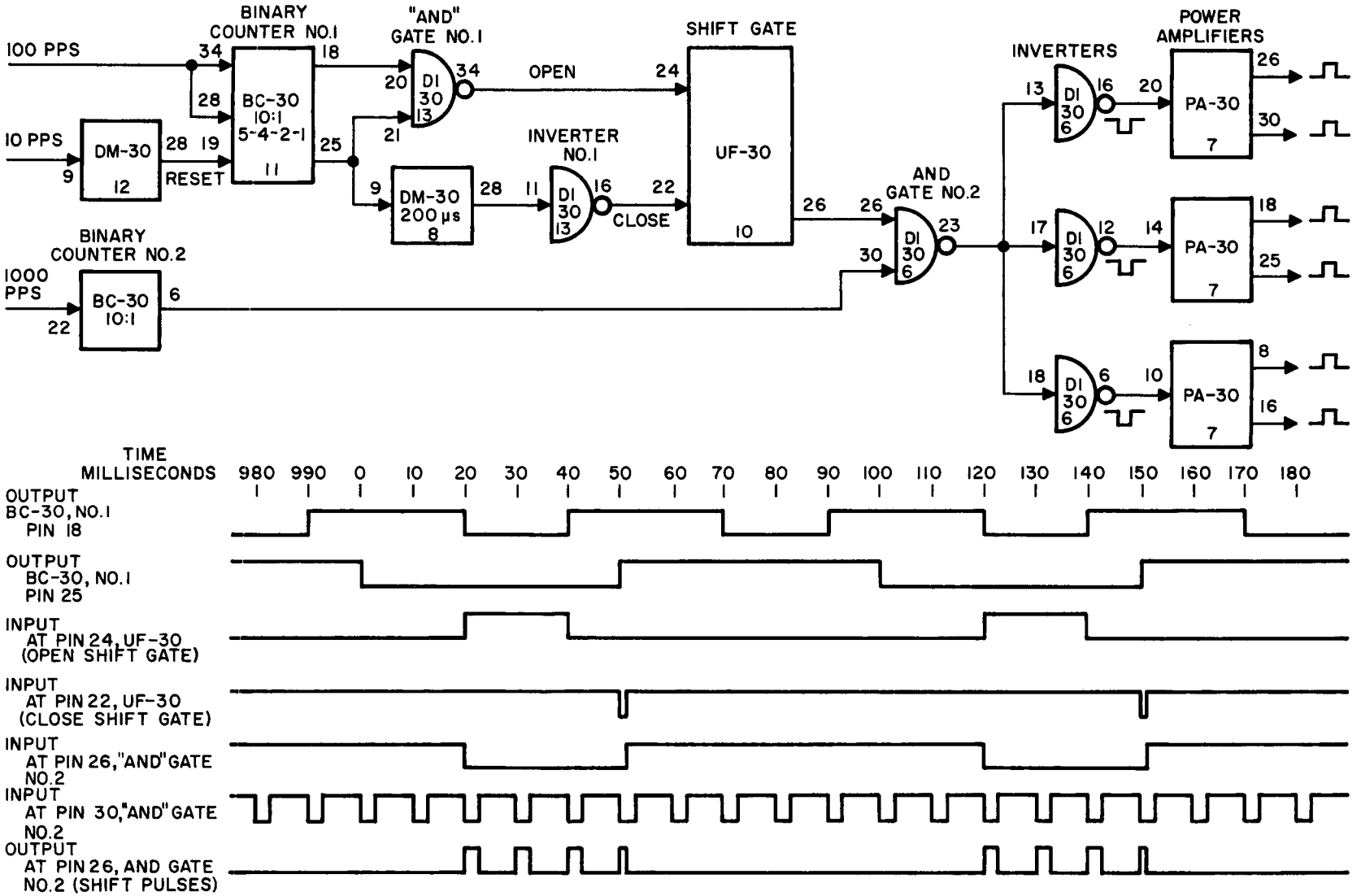


FIGURE 3.17 SHIFT PULSE GENERATOR

2. Circuit Description

For the following discussion, refer to the timing waveforms at the bottom of Figure 3. 17. The output from Pin 18 of binary counter number 1 is applied to Pin 20 of "And" gate number 1. The output from Pin 25 of binary counter number 1 is applied to Pin 21 as the second input to "And" gate number 1 and to Pin 9 of delay multivibrator number 2.

The output from Pin 34 of "And" gate number 1, a positive going 20-millisecond-wide pulse, is applied to Pin 24 (AC Set) of the UF-30, causing the flip-flop to change its state.

The output from Pin 28 of delay multivibrator number 2, a delayed 200-microsecond-wide pulse, is applied to Pin 11 of inverter number 1. The output from Pin 16 of inverter number 1, a negative-going 200 microsecond-wide pulse, is applied to Pin 22 (AC Reset) of the UF-30 causing the flip-flop to change its state.

The output from Pin 26 of the UF-30 is applied to Pin 26 of "And" gate number 2. The other input at Pin 30 of this "And" gate is the 100-pulse-per-second output from Pin 6 of binary counter number 2.

The output from Pin 23 of "And" gate number 2 is four pulses of the 100-pulse-per-second signal.

These four pulses are applied to Pins 13, 17 and 18 of inverters number 2, 3 and 4, respectively. The output from Pins 16, 12 and 6 of these inverters is applied to Pins 20, 14 and 10 of power amplifiers number 1, 2 and 3, respectively.

The output from the power amplifiers, which represent 4 shift pulses, is applied, in parallel, to the 40-stage shift register.

E. Index Marker Generator

1. General

The Index Marker Generator, Figure 3. 18, produces one ten-millisecond-wide pulse every 100 milliseconds, from 100 milliseconds to 900 milliseconds of the time frame. These markers are used to indicate the beginning of a time digit.

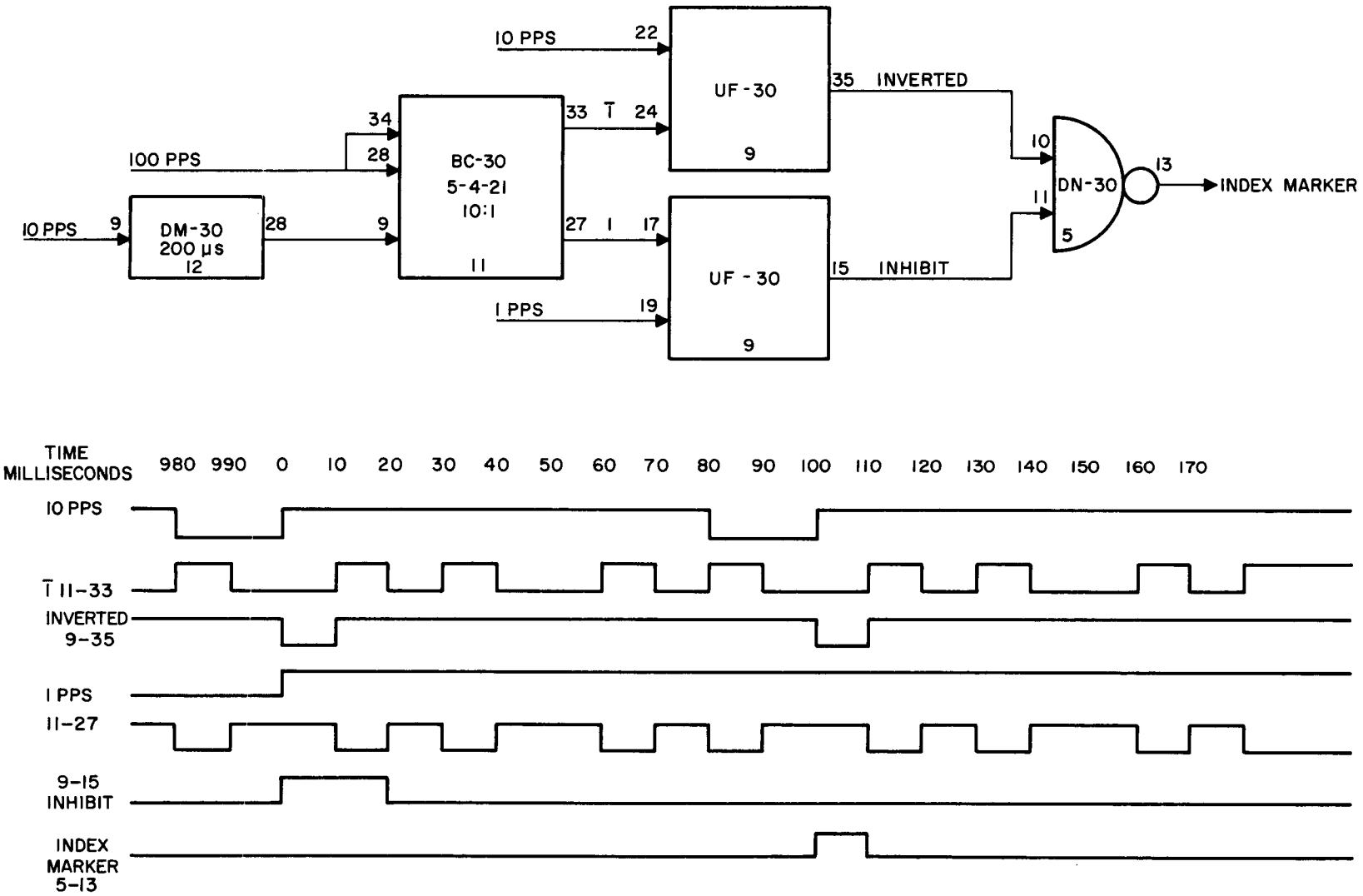


FIGURE 3.18 INDEX MARKER GENERATOR

2. Circuit Description

For the following discussion refer to the waveforms at the bottom of Figure 3.18. The 10-pulse-per-second signal from the Frequency Divider is applied to Pin 22 (AC Reset) of the Universal Flip-Flop (UF-30) number 1. The positive transition (from negative six volts to ground) causes the flip-flop to change its state, causing the output at Pin 35 to fall to a negative six volts.

The $\overline{1}$ one output from Pin 33 of the 5-4-2-1 decade counter (BC-30) is applied to Pin 24 (AC Set) of flip-flop number 1. The positive-going transition of this pulse causes the flip-flop to again change its state, causing the output at Pin 35 (Reset Output) to return to zero volt (ground). This negative 10-microsecond wide pulse is applied to Pin 10 of "And" gate number 1.

The 1 output from Pin 27 of the 5-4-2-1 decade counter is applied to Pin 17 (AC Set) of flip-flop number 2. The positive transition of this pulse will cause the flip-flop to again change its state, causing the output to fall to a negative six volts. This positive 20-millisecond-wide pulse, which is applied to Pin 11 inhibits "And" gate number 1. This pulse, which occurs once each second, prevents the Index Marker from appearing at the beginning of the time frame. However, for the remainder of the time frame the "And" gate is enabled,allowing the Index Marker to appear every 100 milliseconds of the time frame starting at 100 milliseconds through 900 milliseconds.

F. Read Gate Generator

1. General

The Read Gate Generator, Figure 3.19, produces a 40-millisecond-wide pulse that enables the Read Gate,allowing the time information from the Shift Registers to be inserted, at the proper time, in the time frame.

G. Modulator Circuit for Binary Time Code Generator

1. General

The Modulator Circuit Figure 3.20 amplitude modulates a 1-KC carrier in accordance with the dc level changes of the Binary Coded Decimal Time.

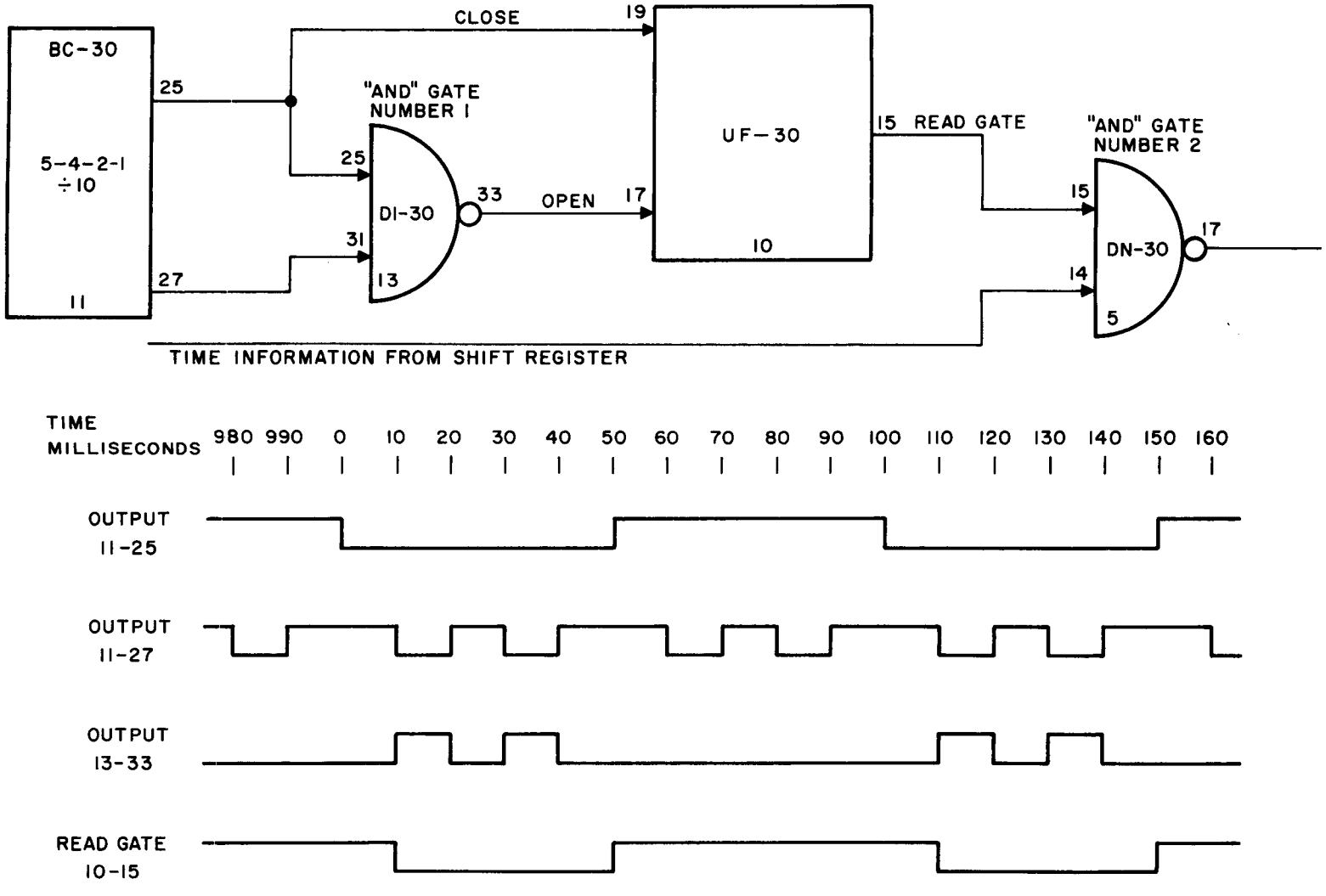


FIGURE 3.19 READ GATE GENERATOR

2. Circuit Description

The 1-KC rectangular wave from the Frequency Divider is applied to the carrier input, Pin 32, through resistor R1 and variable resistor R2 to the tuned circuit composed of inductor L1 and capacitors C1 and C2.

The 1-KC sine wave output from the tuned circuit is coupled through capacitor C3 to the Darlington Emitter-Follower Circuit composed of transistors Q1 and Q2. The Darlington emitter-follower circuit and feedback capacitor C4 prevent the tuned circuit from being overloaded.

The output from the emitter of Q2 is applied to the phase lag network composed of variable resistor R8, resistor R9, and capacitor C5 which allows the zero crossings of the 1-KC carrier to occur in coincidence with the level charges of the Binary Coded Decimal Time. The output from the lag network is buffered by emitter-follower transistor Q3. The coupling network composed of capacitor C6 and resistor R11 removes the dc level from the 1-KC carrier.

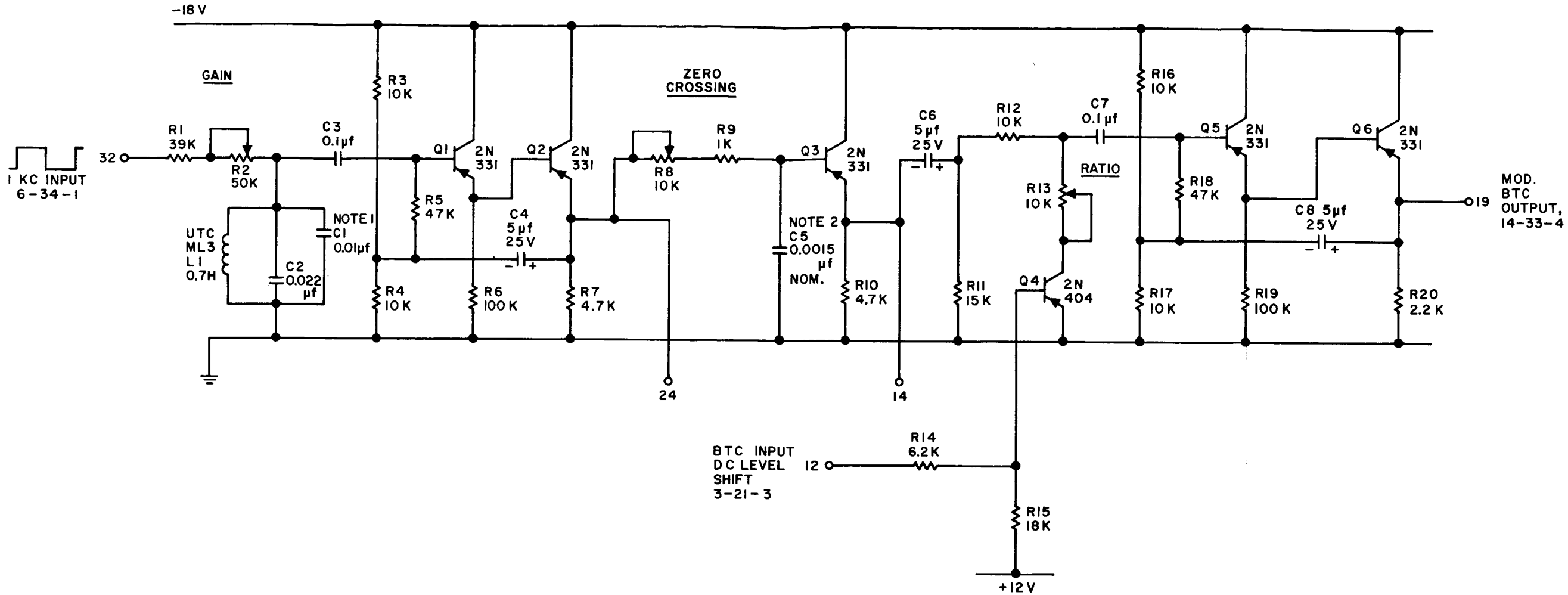
Resistor R12, variable resistor R13, transistor Q4, resistor R14, and resistor R15 compose an impedance modulator. When the Binary Coded decimal time input at Pin 12 is at the zero-volt level, transistor Q4 is cut off allowing the 1-KC carrier to pass through the circuit unattenuated. When the Binary Coded decimal time is at the negative-six-volt (-6) level, transistor Q4 is saturated and the 1-KC carrier is attenuated by the voltage divider network composed of resistor R12 and variable resistor R13. Variable resistor R13 allows the ratio of the two carrier levels to be continuously varied.

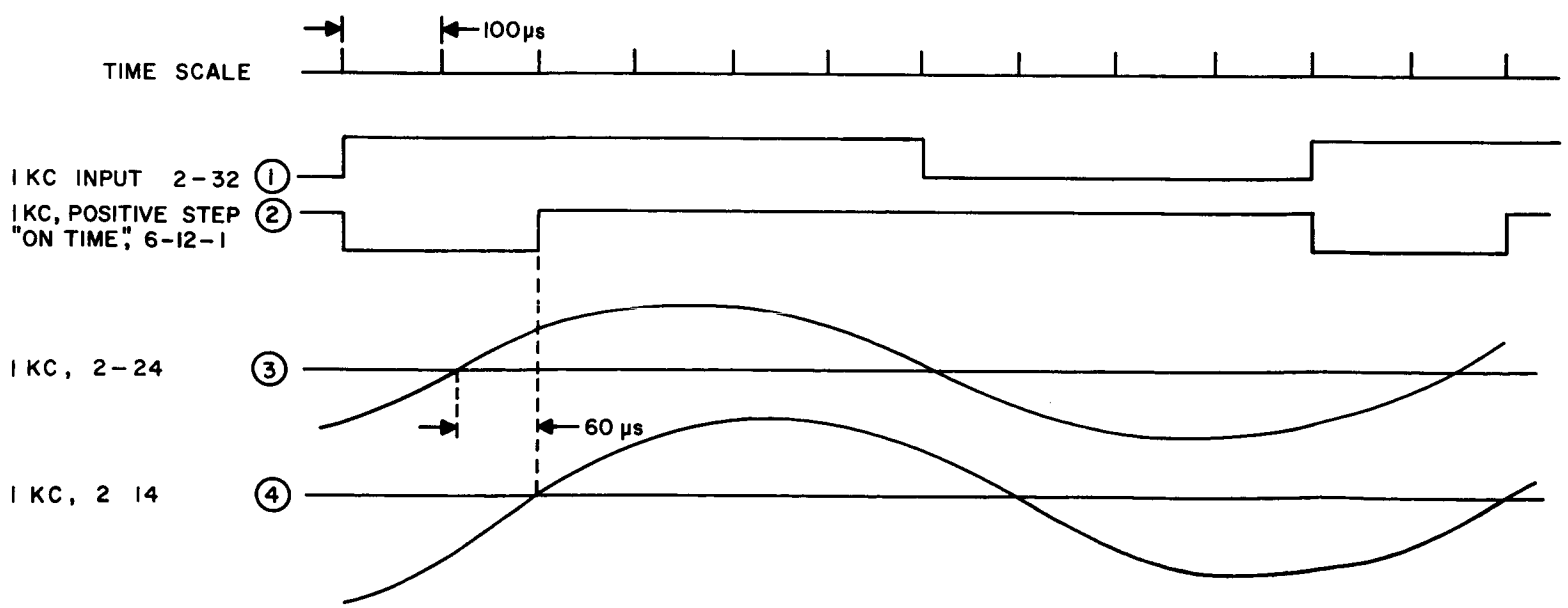
The modulated carrier is coupled through capacitor C7 to the Darlington emitter follower composed of transistors Q5 and Q6. The modulated Binary Coded Decimal output is taken from the emitter of transistor Q6 (Pin 19).

3.10 SIGNAL-DISTRIBUTION CHASSIS

A. General

The signal-distribution chassis receives inputs from the frequency divider, digital clock, and binary time code generator and





NOTES

1. RESONATE AT 1 KC, NOMINAL (DETUNE UNTIL POSITIVE GOING ZERO CROSSING OF 1 KC AT PIN 24 LEADS "ON TIME", 6-12-1, BY APPROXIMATELY 60 μS)

2. SELECT C5 TO ALLOW APPROXIMATELY EQUAL PHASE SHIFT EACH SIDE OF 1 KC "ON TIME" MARK (6-12-1) WHEN R8 IS VARIED FROM MINIMUM TO MAXIMUM.

FIGURE 3.20 MODULATOR CIRCUIT, BINARY TIME CODE GENERATOR

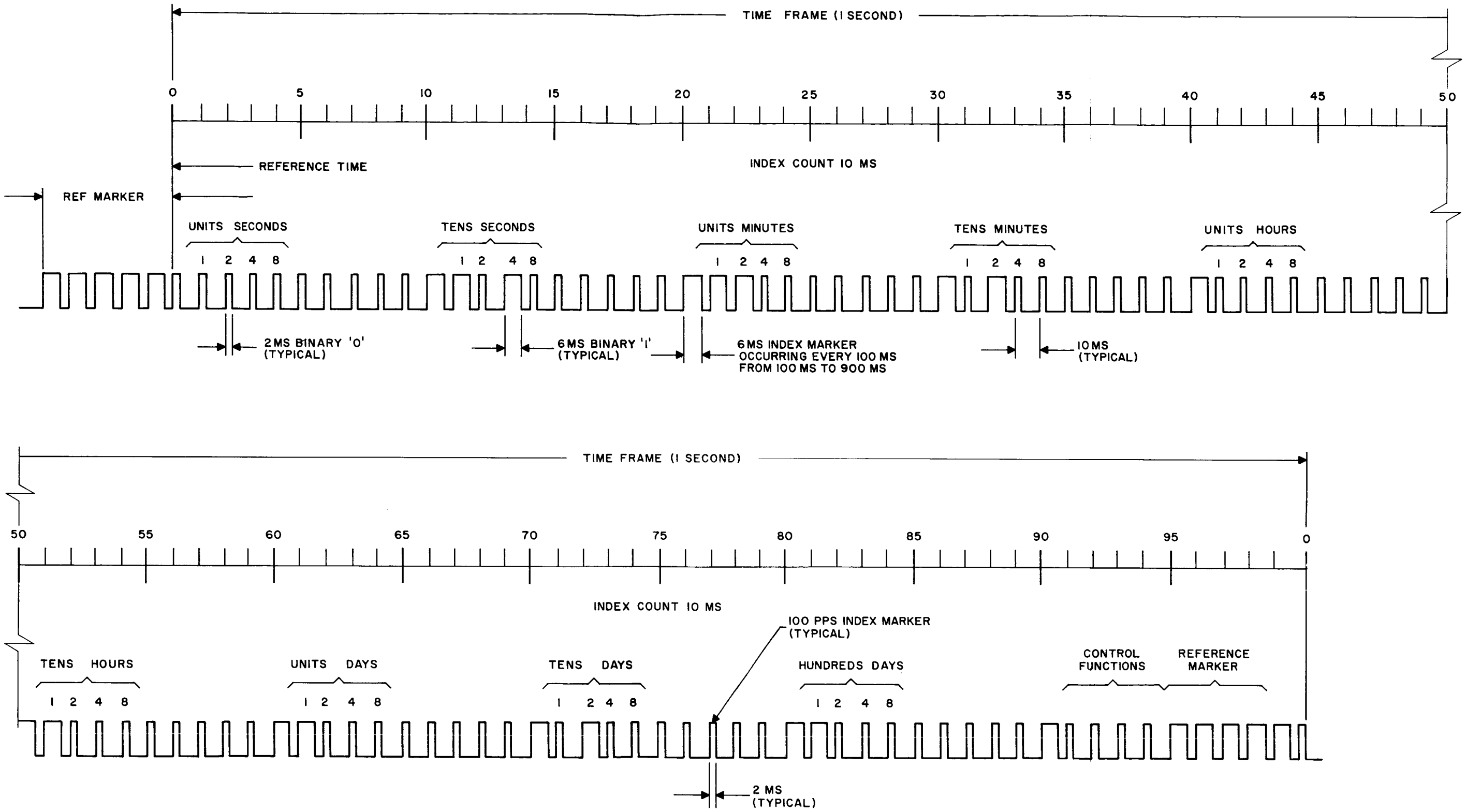


FIGURE 3.21 BINARY TIME CODE FORMAT

distributes these signals to the top panel. It also distributes the time-of-year information to the time-of-year display panel and serves as a buffer between the input and output circuits.

The signal-distribution chassis is composed of standard S-PAC digital modules. The detailed theory of operation of these circuits may be found in section 3 and in the manufacturer's instruction manual referenced in Table 1.1.

B. Block Diagram Description (Figure 3.22)

A 1-megacycle 6-4 wave from pin 10 card 1 (MC-30) in the frequency divider is fed to pin 14 of power-amplifier card 1 (PA-30) located in the signal-distribution chassis. The common outputs from pins 18 and 25 are fed through J 20 on the patch panel to J 20 on the top panel.

The 500-KC 6-4 pulse output from pin 25 of decade-counter card 2 (BC-30) is coupled to pin 29 of buffer-inverter card 14 (DI-30) located in the frequency divider. The output from pin 27 is fed to pin 20 of power-amplifier card 1 (PA-30) located in the signal-distribution chassis. The common outputs from pins 26 and 30 are fed through J 19 on the patch panel to J 19 on the top panel.

The 10-pulse-per-second signal from pin 6 of decade-counter card 9 (BC-30) is coupled to pin 18 of buffer-inverter card 6 (DI-30) located in the frequency divider. The output from pin 6 is fed to pin 9 of buffer-inverter card 20 (DI-30) located in the signal-distribution chassis. The output from pin 7 is applied in parallel to pins 9 and 11 of buffer-inverter card 16 (DI-30). The output from pin 16 is applied to pins 14 and 20 of power-amplifier card 18 (PA-30), and the output from pin 7 is applied to pin 10 of power-amplifier card 17 (PA-30). The common outputs from pins 26 and 30, 18 and 25,and 8 and 16 are fed through J 7, J 8, and J 9 on the patch panel, respectively, to J 7, J 8, and J 9 on the top panel.

The 1-pulse-per-second signal from pin 9 of decade-counter card 11 (BC-30) is coupled to pin 9 of buffer-inverter card 14 (DI-30) located in the frequency divider. The output from pin 7 is fed in parallel to pins 18 and 26 of buffer-inverter card 20 (DI-30) located in the signal-distribution chassis. The output from pin 23 is applied in parallel to pins 10 and 22 of power-amplifier cards 18 and 19 (PA-30), respectively, and the output from pin 6 is applied

to pin 10 of power-amplifier card 18 (PA-30). The common outputs from pins 8 and 16, 32 and 35, and 8 and 16 are fed through J 4, J 5, and J 6 on the patch panel, respectively, to J 4, J 5, and J 6 on the top panel.

The units-of-seconds time information from decade-counter card 12 (BC-30) and the tens-of-seconds time information from decade-counter card 13 (BC-30) are applied in parallel to buffer-inverter card 15 (DI-30), located in the frequency divider. The output from these buffer inverters is fed through buffer-inverter cards 20 and 21 (DI-30) located in the signal-distribution chassis to the units-of-seconds and tens-of-seconds indicators located on the clock-amplifier panel.

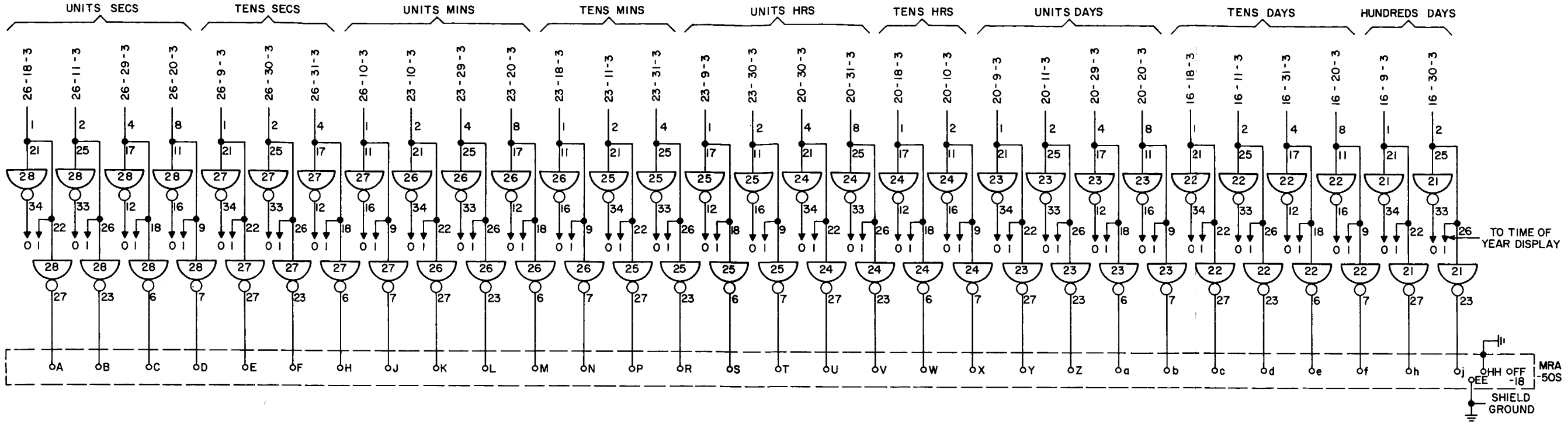
The time-of-year information in parallel from the binary time code generator is applied through buffer-inverter cards 21 to 28 to the time-of-year display panel and to the top panel.

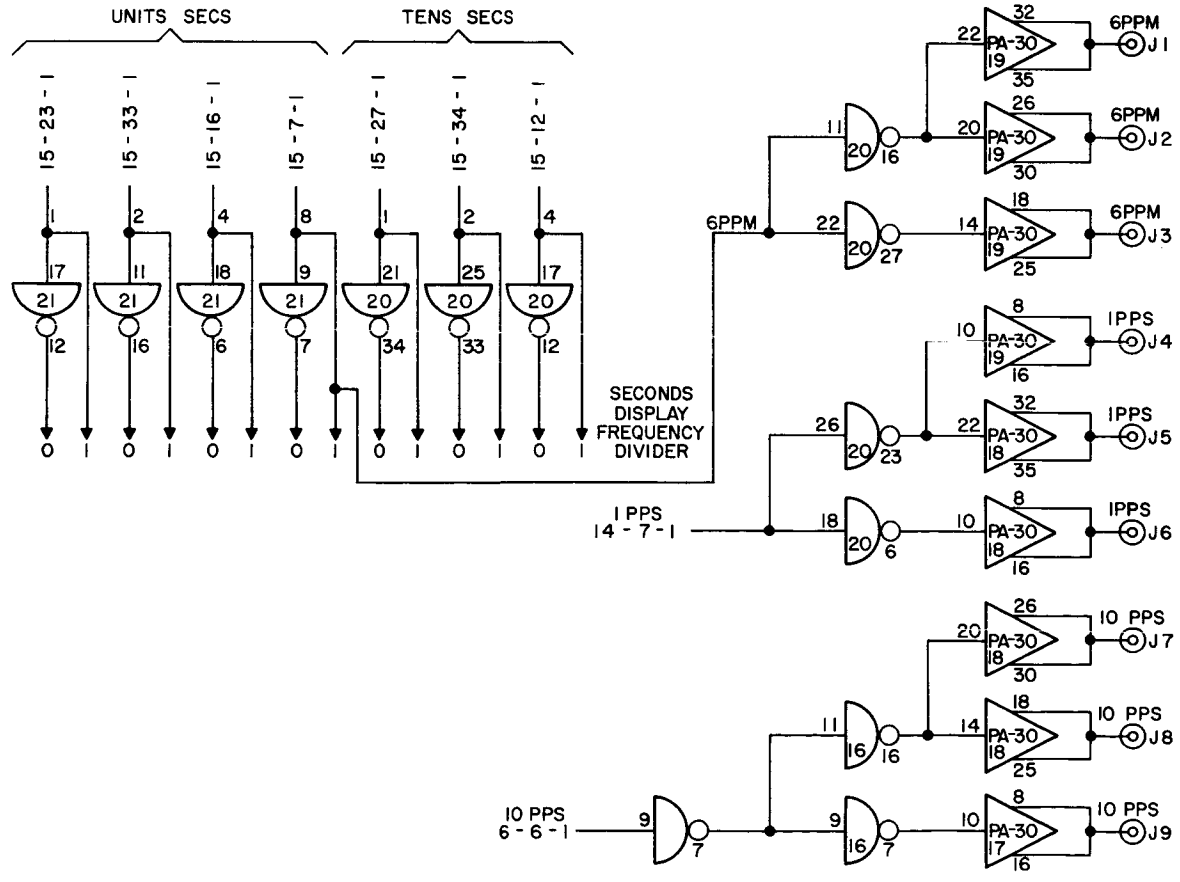
The modulated serial decimal time code from the serial decimal time code generator is applied to pin 25 of emitter-follower card 14 (SC-30F) located in the signal-distribution chassis. The outputs from pins 21 and 23 are fed through J 16 and J 17 on the patch panel, respectively, to J 16 and J 17 on the top panel.

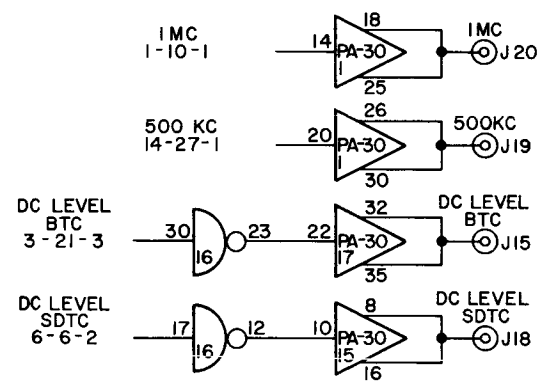
The DC level shift serial decimal time code from the serial decimal time code generator is applied to pin 17 of buffer-inverter card 16 (DI-30) located in the signal-distribution chassis. The output from pin 12 is applied to pin 10 of power-amplifier card 15 (PA-30). The common outputs from pins 8 and 16 are fed through J 18 on the patch panel to J 18 on the top panel.

The modulated binary time code from the binary time code generator is applied to pins 33 of emitter-follower card 14 (SC-30F) located in the signal-distribution chassis. The outputs from pins 31 and 28 are fed through J 13 and 14 on the patch panel, respectively, to J 13 and J 14 on the top panel.

The DC level shift binary time code from the binary time code generator is applied to pin 30 of buffer-inverter card 16 (DI-30) located in the signal-distribution chassis. The output at pin 23 is applied to pin 22 of power-amplifier card 17 (PA-30). The common outputs from pins 32 and 35 are fed through J 15 on the patch panel to J 15 on the top panel.







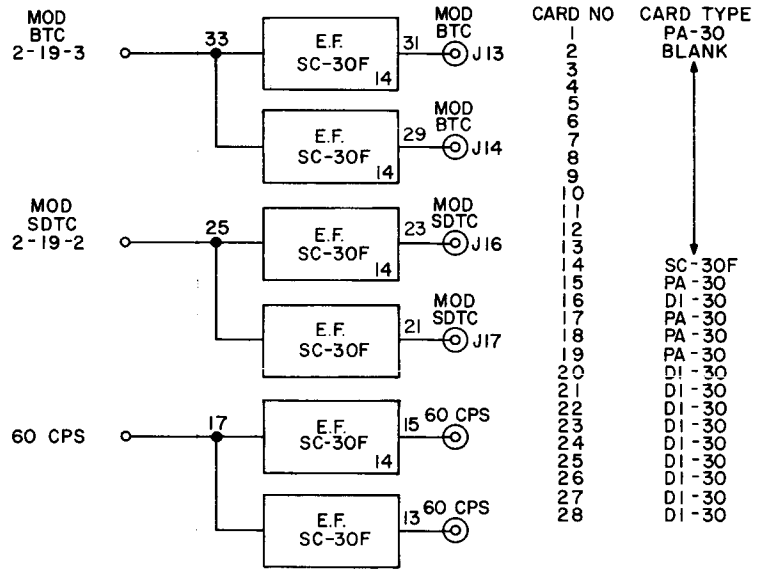


FIGURE 3.22 - SIGNAL-DISTRIBUTION CHASSIS

The power amplifier, PA-30, is capable of driving a 90-ohm line and should be terminated with a 90-ohm impedance. This configuration allows for a rise and fall time of the order of 0.2 microsecond. The amplitude is attenuated from 6 volts to 4.5 volts.

3.11 POWER CIRCUITS

A. General

Power is supplied to the time standard from two primary sources: (1) a 115-volt 60-cps power source, and (2) a 28-volt nickel-cadmium battery. The battery is used as the emergency supply. During normal operations the battery remains connected to the emergency power supply filter network and is subjected to a very slow charge current.

In the following discussion the power circuit is divided into four parts: (1) the 115-volt 60-cps power circuit, (2) the primary dc power supply, (3) the indicator power supply, and (4) the emergency power supply.

B. Power Control

The two primary power sources are controlled from the power control panel and the emergency power transfer panel.

The power control panel contains a manually operated ac circuit breaker designated "AC POWER." When this switch is placed in the "ON" position, power is applied to the time standard rack. The panel also contains a "voltage monitor" switch and an associated dc voltmeter that allows the dc voltages from the RP-32 power supply to be metered.

The emergency power control panel contains a toggle switch designated "AC POWER." When this switch is placed in the "ON" position, power is applied to the emergency power supply. This panel also contains a "VOLTAGE MONITOR" switch and an associated dc voltmeter that allow the dc voltage from the emergency power supply to be metered.

The interrack power cabling is shown in Figure 3.23.

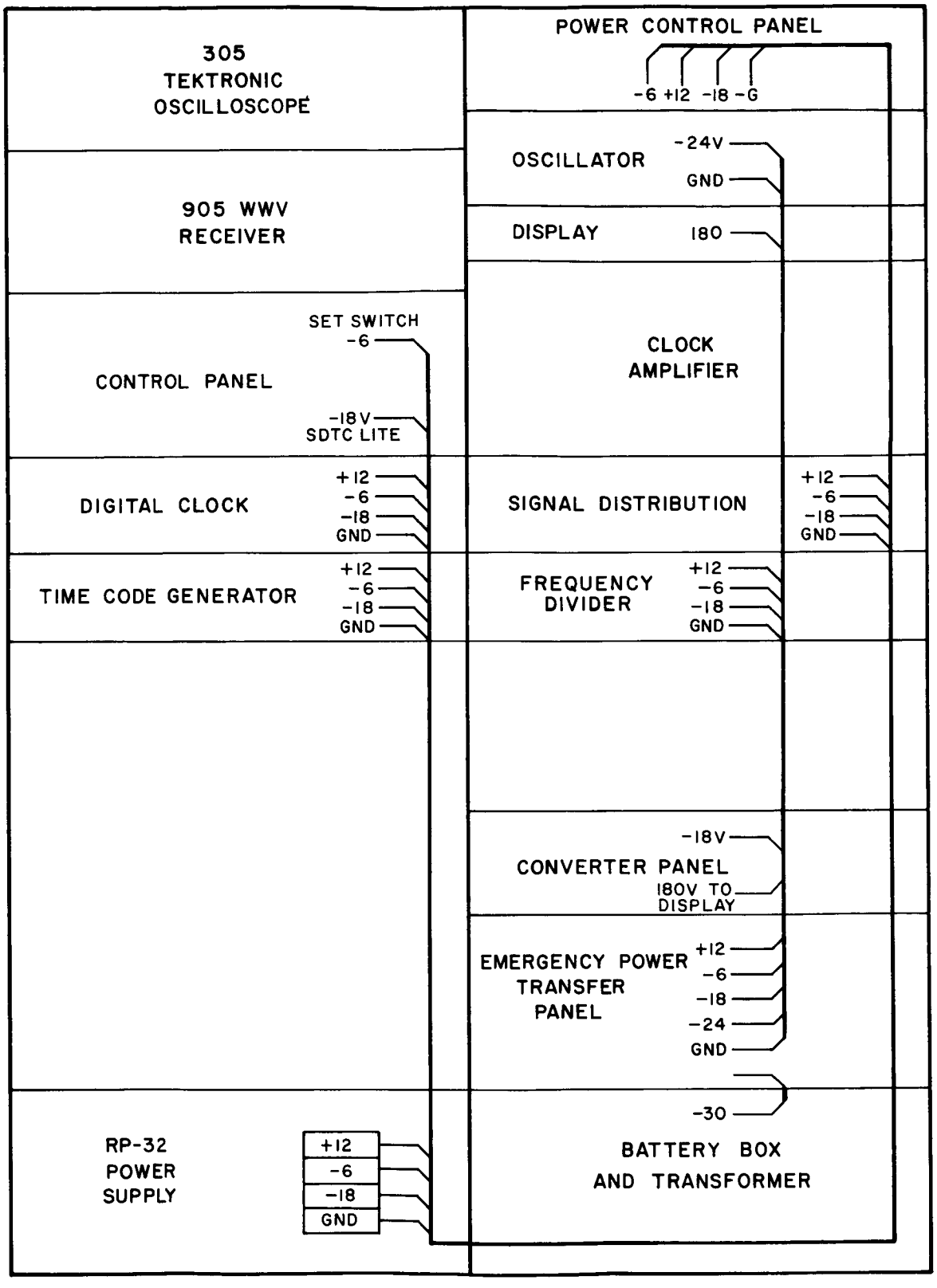


FIGURE 3.23 INTERRACK CABLING

C. 115-Volt AC Power Circuit

The 115-volt ac power circuit is shown in Figure 3.24. When the time standard is connected to a 115-volt 60-cps power source, power is applied to the blowers located at the top of each cabinet. When the "AC POWER" switch (15-amp circuit breaker) is placed in the "ON" position, power is applied to the elapsed timing meter and to five service outlets to which the 503 Tektronic Oscilloscope, the WWV receiver, the indicator power supply, the RP-32 power supply, and the emergency power supply are connected.

D. Primary Power Supply

The primary power supply is shown in the block diagram of Figure 3.25. The RP-32 power supply furnishes power to the control panel, the binary time code generator, the digital clock, the signal-distribution chassis, and the power control panel.

The theory of operation of the RP-32 power supply can be found in the manufacturer's instruction manual referenced in Table 1.1.

E. Indicator Power Supply

1. General

The indicator power supply is shown in the block diagram of Figure 3.26. This supply consists of the ERA Transpac Model TR 200 M or the Dresson Barnes Model 30-200 power pack which supplies 180 volts dc to the time-of-year and seconds indicators and 200 volts dc to the time comparison circuit, card 16, located in the frequency divider.

2. Circuit Description

The ERA Transpac Model TR 200 M power pack combines the properties of a magnetic controller with the fast response of a transistor regulator. Preregulation and line transit protection is achieved by the magnetic controller. The supply will provide zero output in the event of excessive current flow due to overload or a short in the external circuit. The transistor regulator accommodates all fast line or load variations and transients and provides for ripple reduction. Under short-circuit conditions, substantially

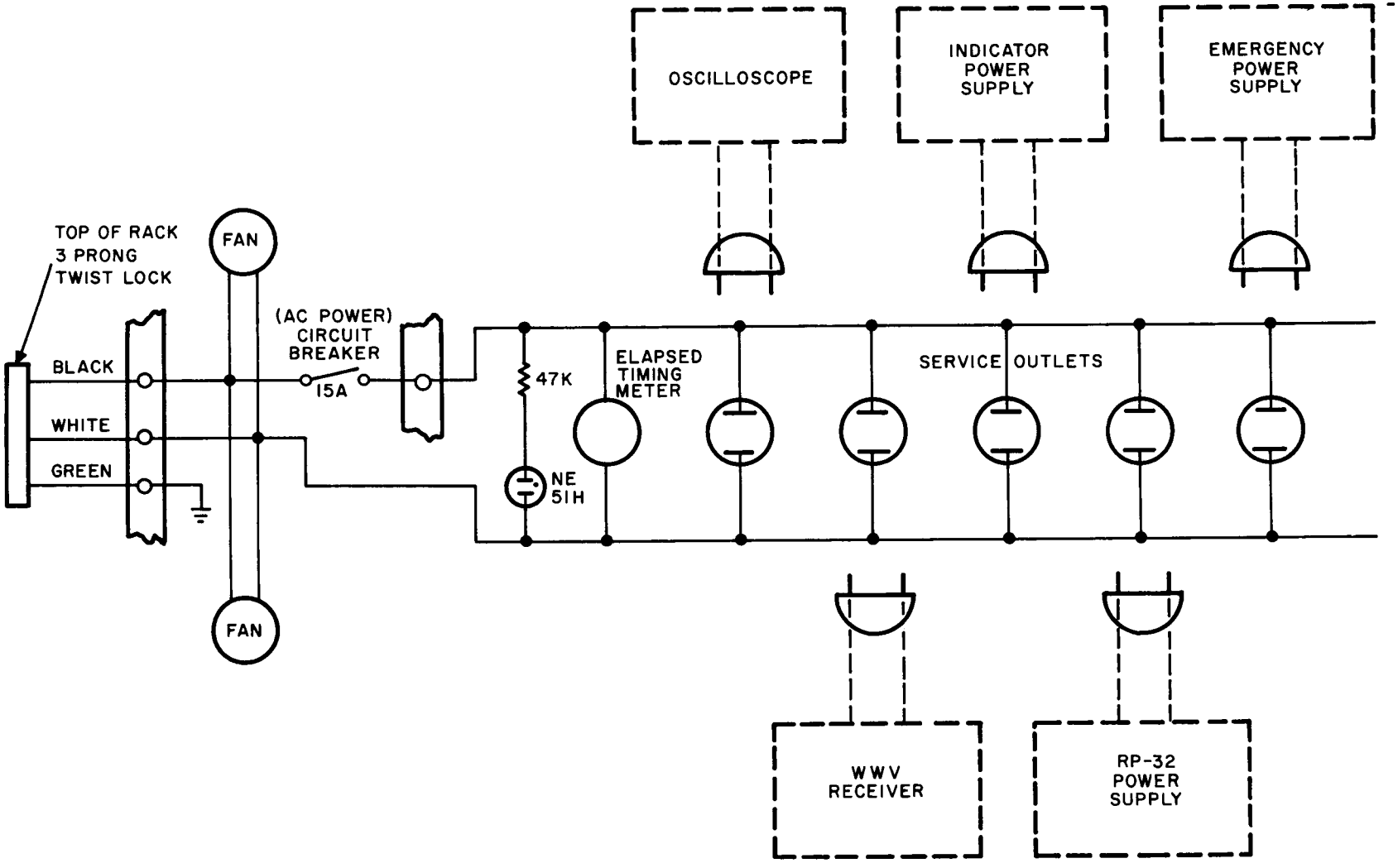


FIGURE 3.24 AC POWER CIRCUIT

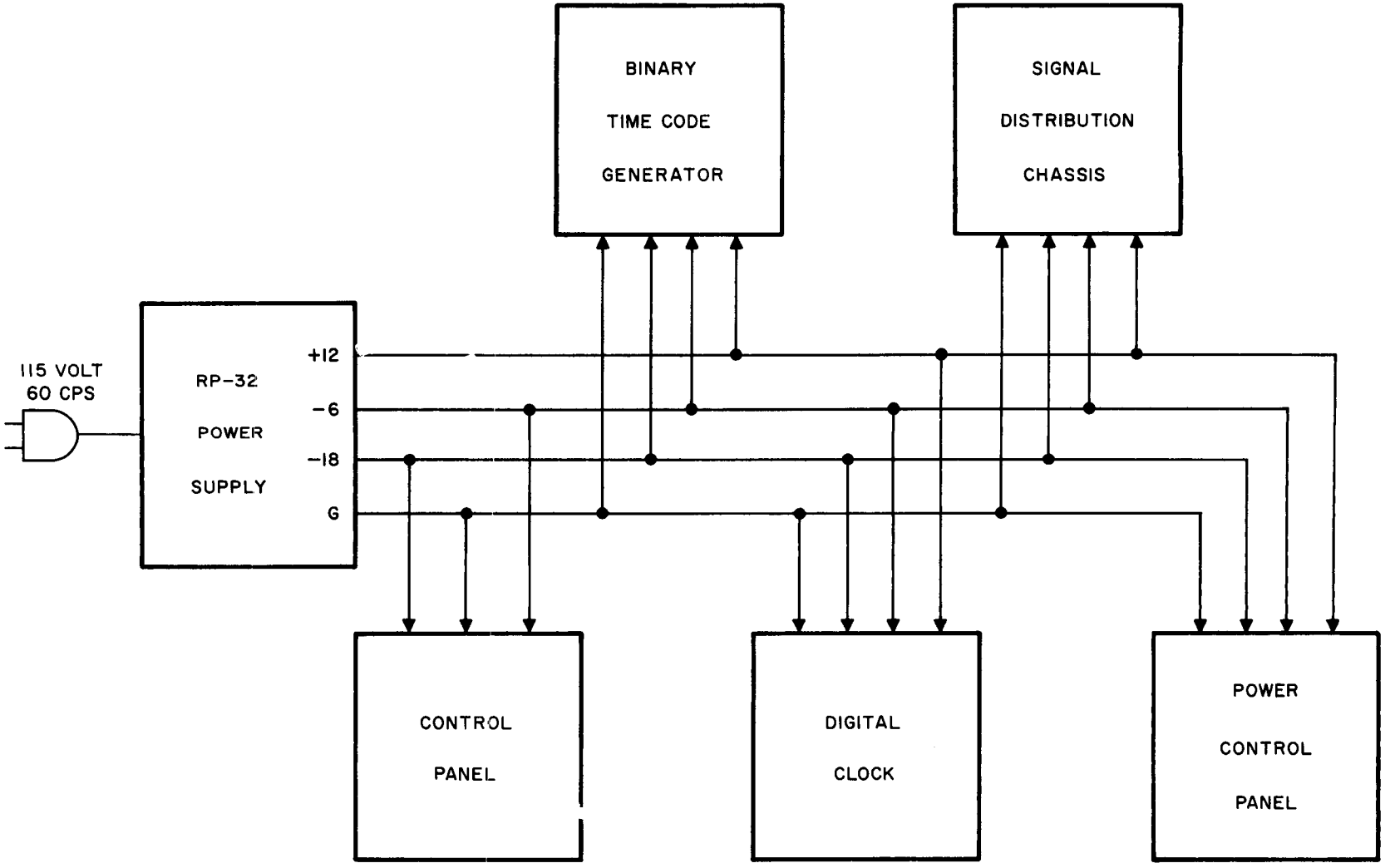


FIGURE 3.25 PRIMARY DC POWER CIRCUIT

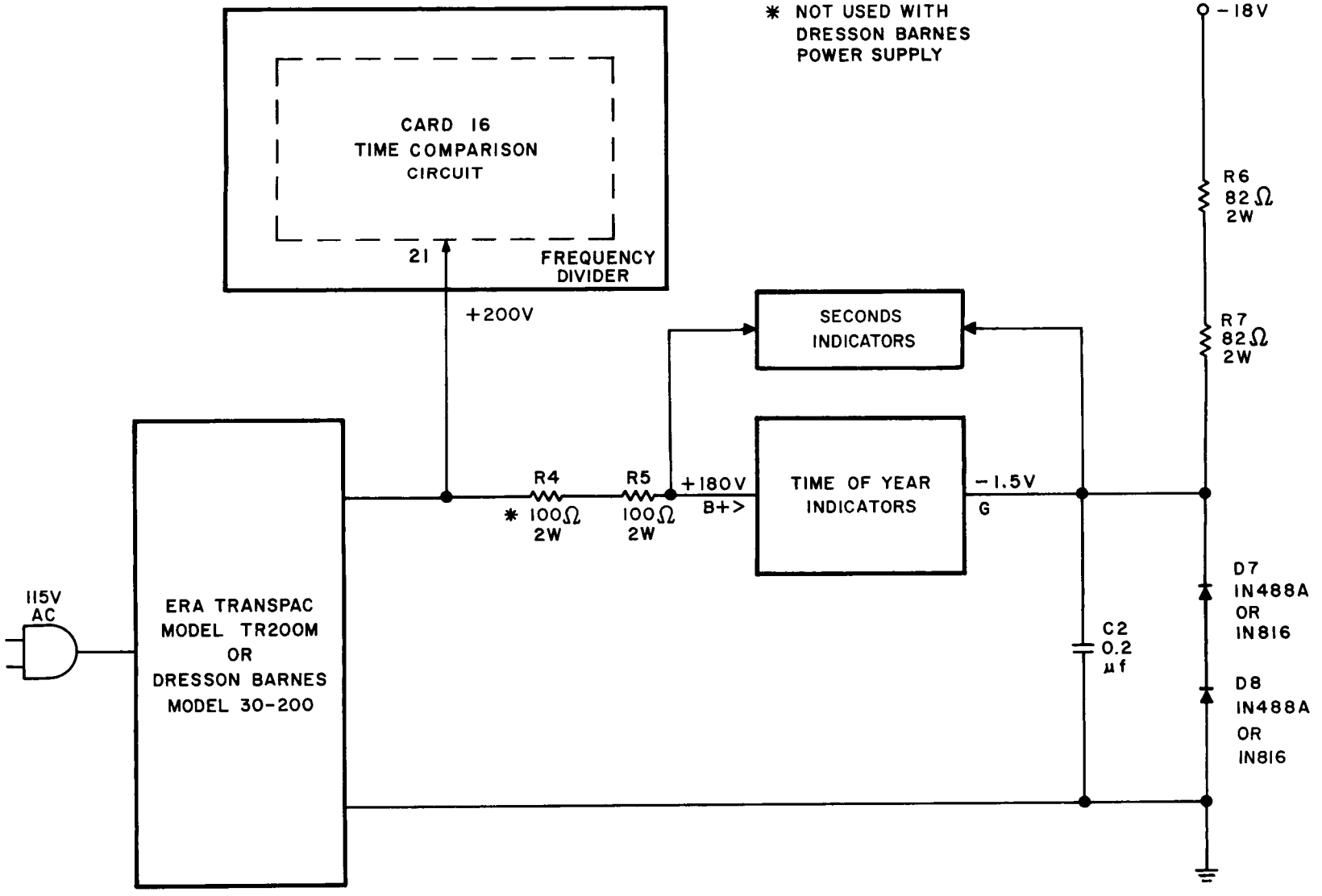


FIGURE 3.26 INDICATOR POWER SUPPLY

zero voltage appears across the transistors and there is minimum heat dissipation.

F. Emergency Power Supply

1. General

The emergency power supply furnishes well regulated dc voltages to the frequency divider, the HP 104 AR oscillator, and the 60-cps generator amplifier circuit.

Under normal conditions the power supply is connected to the 115-volt 60-cps power source; however, if the 115-volt 60-cps power should fail, power will be supplied from the 28-volt nickel-cadmium battery. This switchover is accomplished automatically and without any power interruption.

2. Block-Diagram Description

The emergency power supply is shown in the block diagram of Figure 3.27. The 115-volt 60-cps power is applied through switch S1 and the full-wave bridge rectifier to the filter network. During normal operation, the output from the filter network is coupled through variable resistor R7 and diode CR7 to the junction of diodes CR7 and CR8. The variable resistor R7 is adjusted for a voltage of 30 volts at the junction of the two diodes.

The output from the junction of diodes CR7 and CR8 is applied in parallel to the 18-volt regulating network, to the HP 104 AR oscillator, and through the Sorenson QC convertor to the 12-volt regulating network.

The diodes CR7 and CR8 serve as gates. The voltage which is more negative at the input to the diodes determines which power supply furnishes the load current.

When the ac power fails the voltage at CR8 is more negative and the battery is switched to the load.

The output from the 18-volt regulating network is applied in parallel to the 6-volt regulating network and to pins 1 and 8 of the IT-226A ERA dc/ac inverter located on the converter panel.

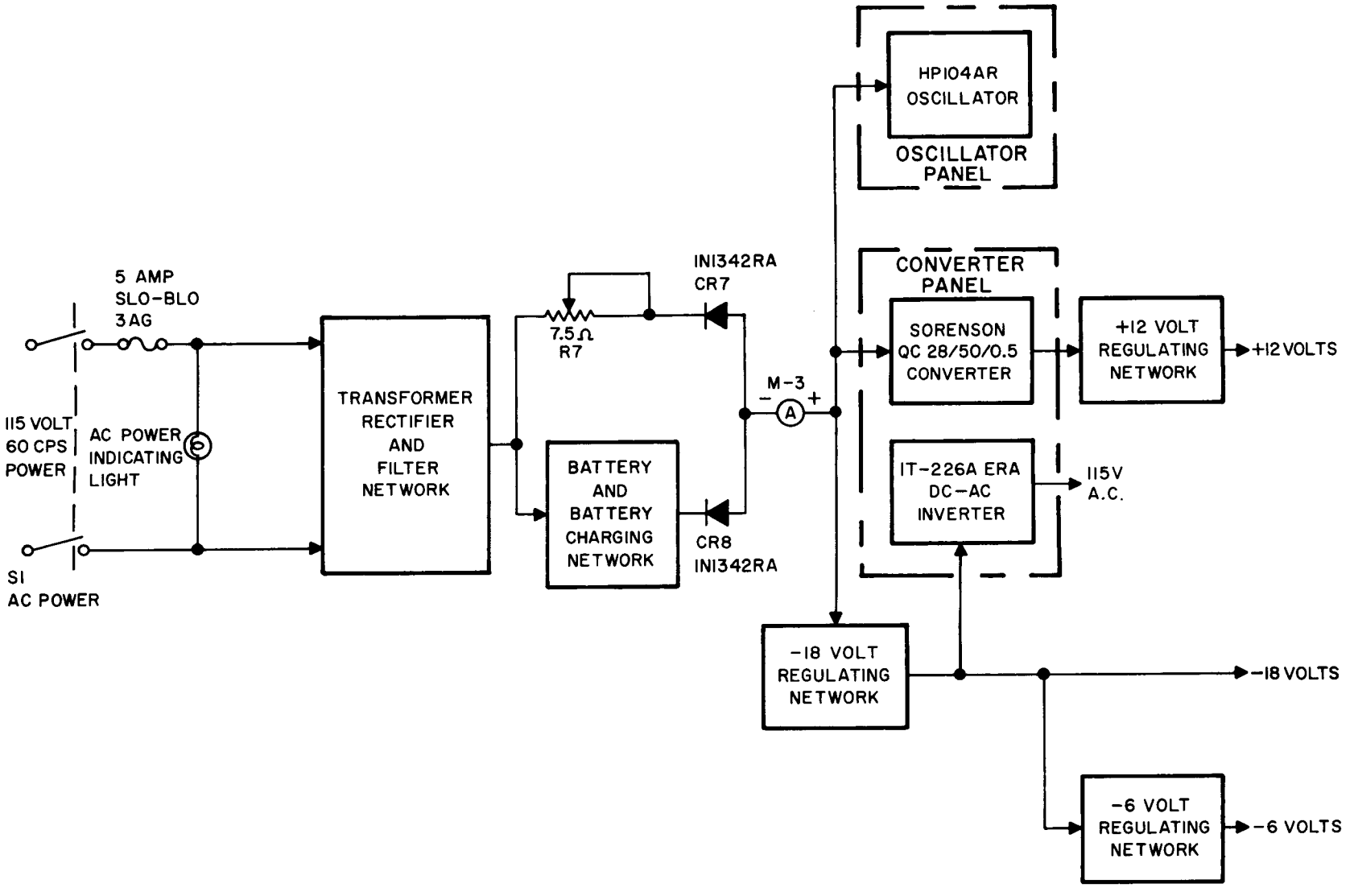


FIGURE 3.27 EMERGENCY POWER SUPPLY BLOCK DIAGRAM

3. Circuit Description

The partial schematic diagram shown in Figure 3.28 is used to explain the operation of the battery charging circuit and the 18-volt regulating network. The regulating circuit operates by controlling the regulator impedance in series with the load. Here the regulating impedance is a transistor which is controlled by comparing the voltage across the load with a reference voltage, amplifying any difference in the compared values, and applying this difference to the regulating transistor. The end result is a closed loop in which the load current is proportional to the differences between the measured load voltage and the reference voltage.

Diode CR9, which is located in the emitter of transistor Q5, determines the reference voltage, and resistor R11 limits the current through diode CR9 to nearly a constant current. The combination of resistor R12, variable resistor R14, and resistor R13 compose the output sensing network, a portion of which is compared by transistor Q5 with the voltage across diode CR9. The portion of the output voltage being compared determines the bias on transistor Q5. Any difference in the compared voltage is amplified by transistors Q5 and Q4 and is applied to transistor Q3 where it is amplified and used as an output control.

A preregulator is incorporated to prevent any ripple from being amplified and appearing in the output. The preregulator consists of resistors R9 and R10 and the zener diode CR10. The zener diode functions to provide a constant voltage across resistor R10 and a constant current to transistors Q5 and Q4. Thus, any variation (ripple) of the input voltage will be prevented from being amplified and appearing at the output of the power supply.

Under normal conditions switch S2 is in the "normal charge" position and the charging current for the battery is supplied through variable resistor R5 and resistor R6. Resistor R5 is adjusted until meter M1 reads 100 milliamperes.

Periodically, or after the battery has been used to supply power to the time standard, it is desirable to charge the battery at a high rate; switch S2 must then be set in the "fast charge" position. With switch S2 in the "fast charge" position, charging current for the battery is supplied through variable resistor R3 and resistor R4. Resistor R3 is adjusted until meter M1 reads 1 ampere.

NOTE

Do not allow the charge rate switch to remain in the high-charge position for more than an 8-hour period, or the battery will be permanently damaged.

The zener diode CR5 and transistors Q2 and Q1 are used to provide a constant 6 volts across the resistance network.

A transistorized converter, manufactured by Sorenson and Co., Inc., is used to help develop the positive 12-volt supply from the emergency power supply. For the following discussion refer to Figure 3.29.

The action of the inverter is similar to that of a multivibrator. When the input voltage is applied, transistor Q1 starts to conduct because of an unbalance in the circuit. This action results in the input voltage being applied across winding N1 of transformer T1.

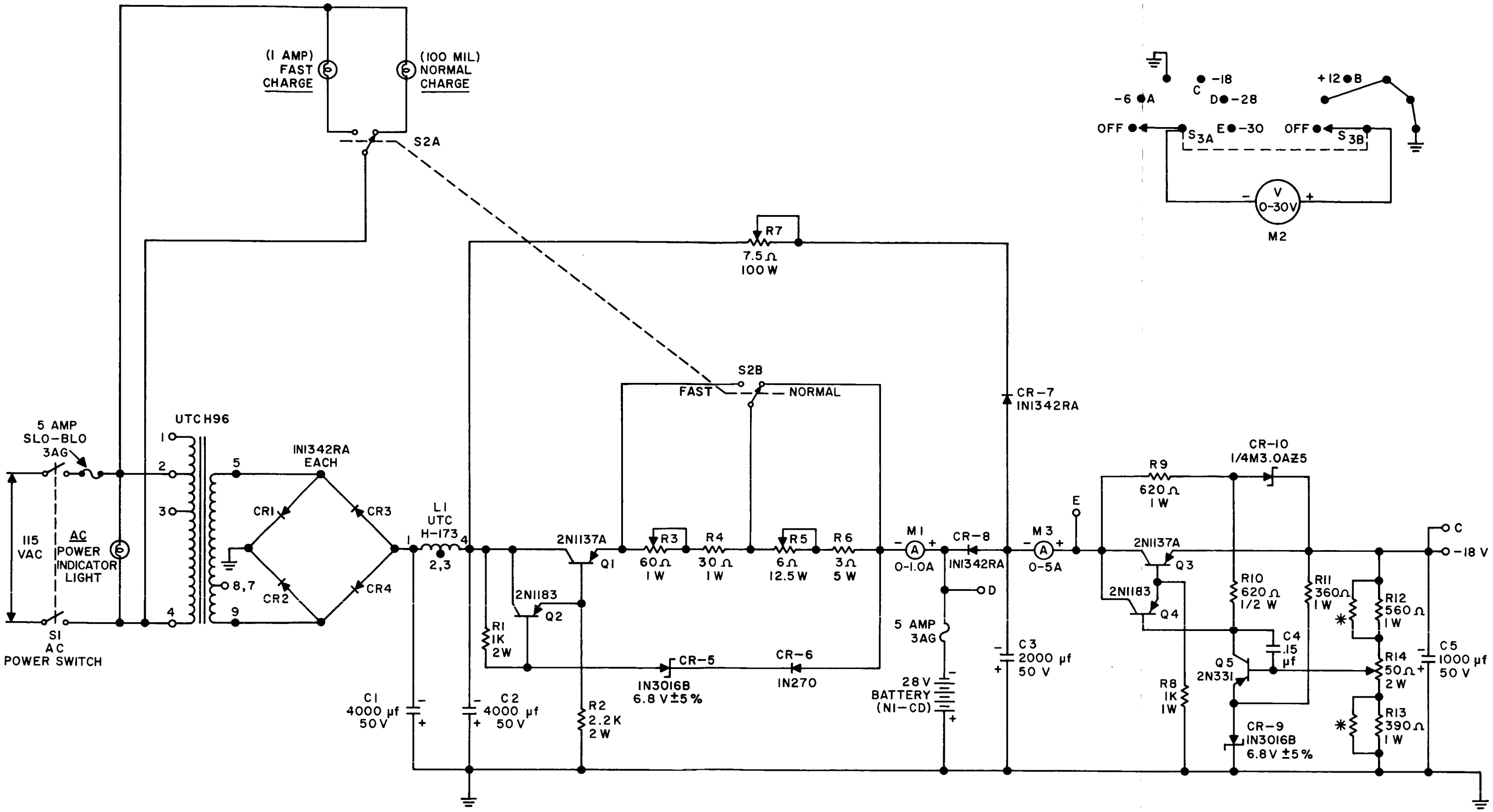
The voltage across winding N1 produces a flux change in the core which induces a voltage across the transistor control windings N3 and N4 and causes Q1 to conduct more and Q2 to block more. This condition exists until the core reaches its saturation point; then the rate of flux change falls to zero, thereby removing the voltages from the control windings N3 and N4. The loss of voltage across winding N3 opens transistor Q1 and so removes the voltage from winding N1. The core then resets itself to its retentive value which corresponds to a small flux change in the reverse direction.

As the core resets itself a small voltage is induced across control windings N3 and N4 which causes transistor Q2 to conduct and transistor Q1 to block. These conditions repeat at a rate directly proportional to the voltages and inversely proportional to flux saturation.

A stepped-up square-wave voltage at the aforementioned rate will then appear across winding N5. This square wave is then rectified, filtered, and applied to the 12-volt regulating network.

3.12 SIGNAL DEVELOPMENT DIAGRAMS

The signal development diagrams, Figures 3.30 to 3.37, have been developed in order to provide the technician with an efficient guide in following the signals through the various units of the time standard rack. They provide a quick and accurate method of isolating any signal discrepancy in a particular unit.



NOTE :
* SELECTED FOR PROPER OUTPUT VARIATION

FIGURE 3.28 EMERGENCY POWER SUPPLY, PARTIAL SCHEMATIC

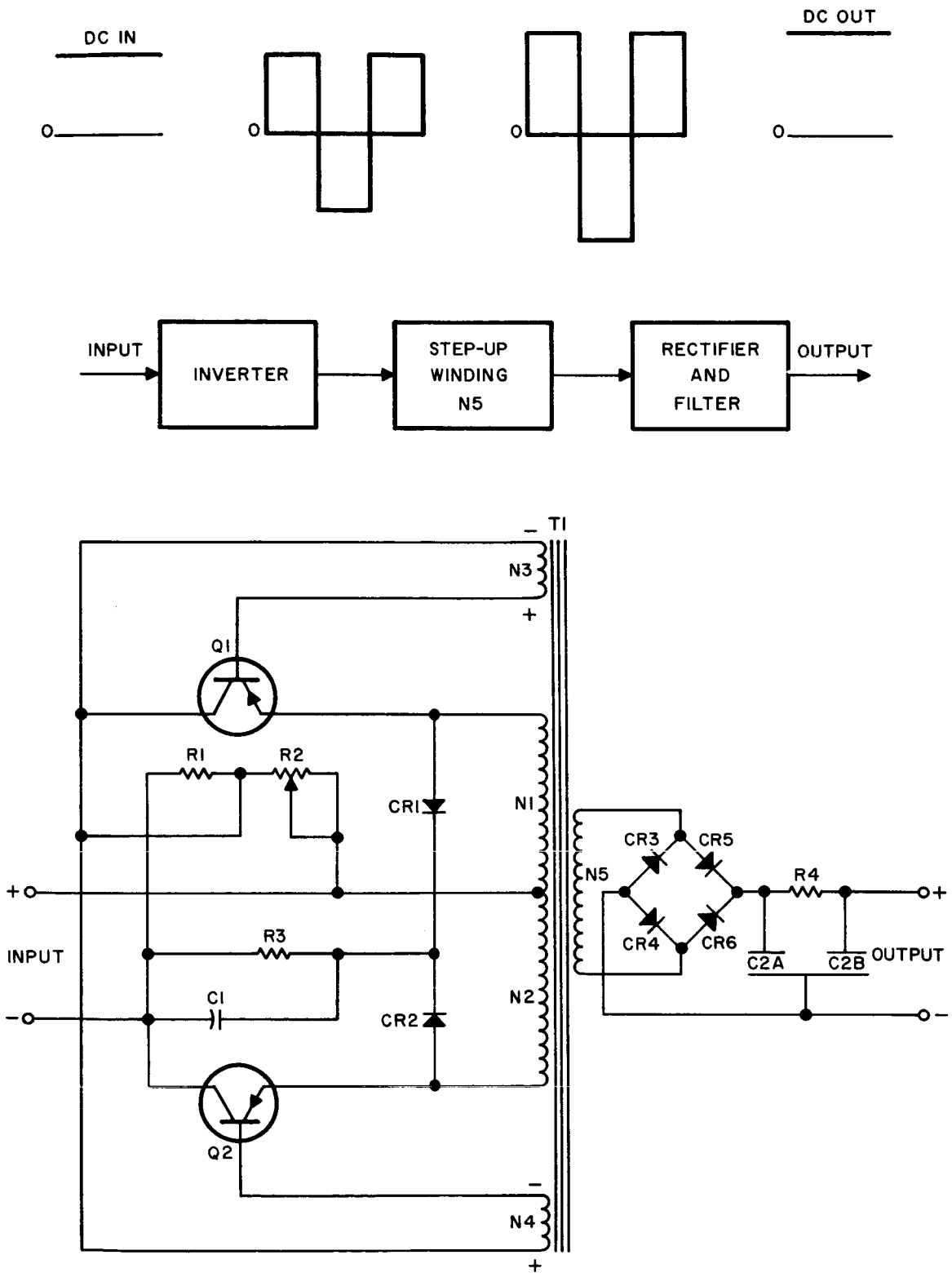


FIGURE 3.29 SORENSON QC 28/50/0.5 CONVERTER

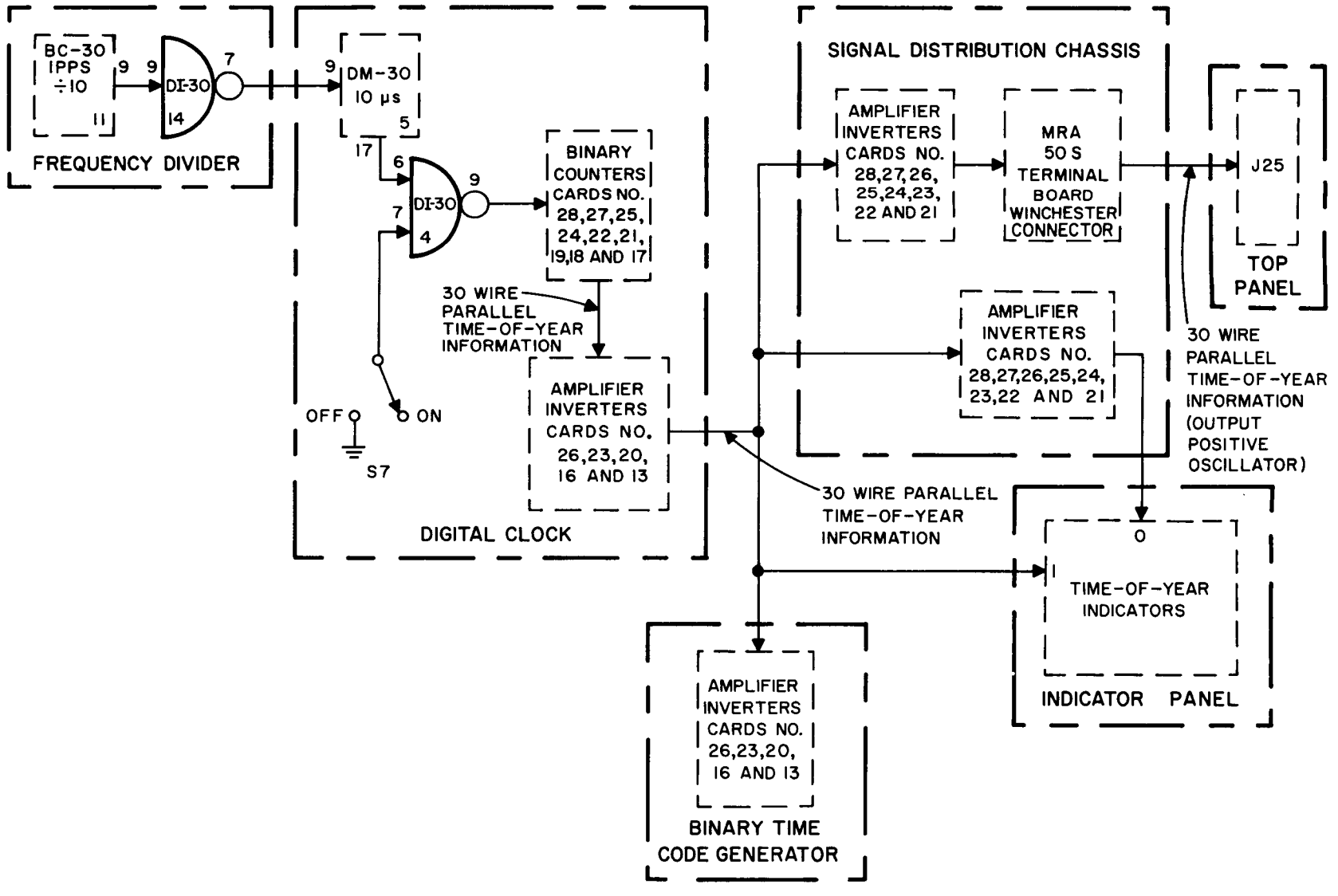


FIGURE 3.30 30-WIRE PARALLEL TIME-OF-YEAR, SIGNAL DEVELOPMENT

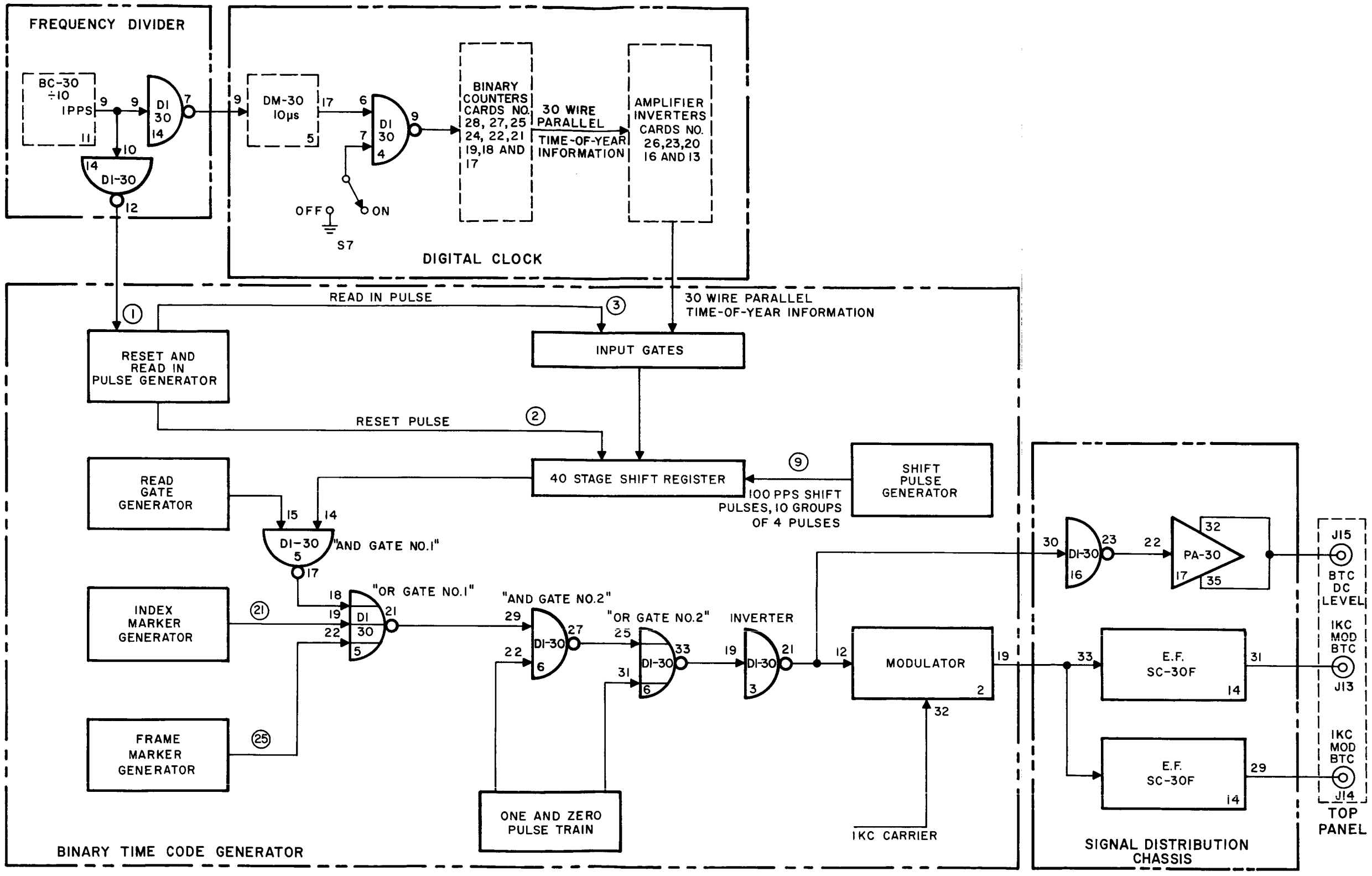


FIGURE 3.31 NASA 100-PPS BINARY TIME CODE SIGNAL DEVELOPMENT (1/Sec BTC)

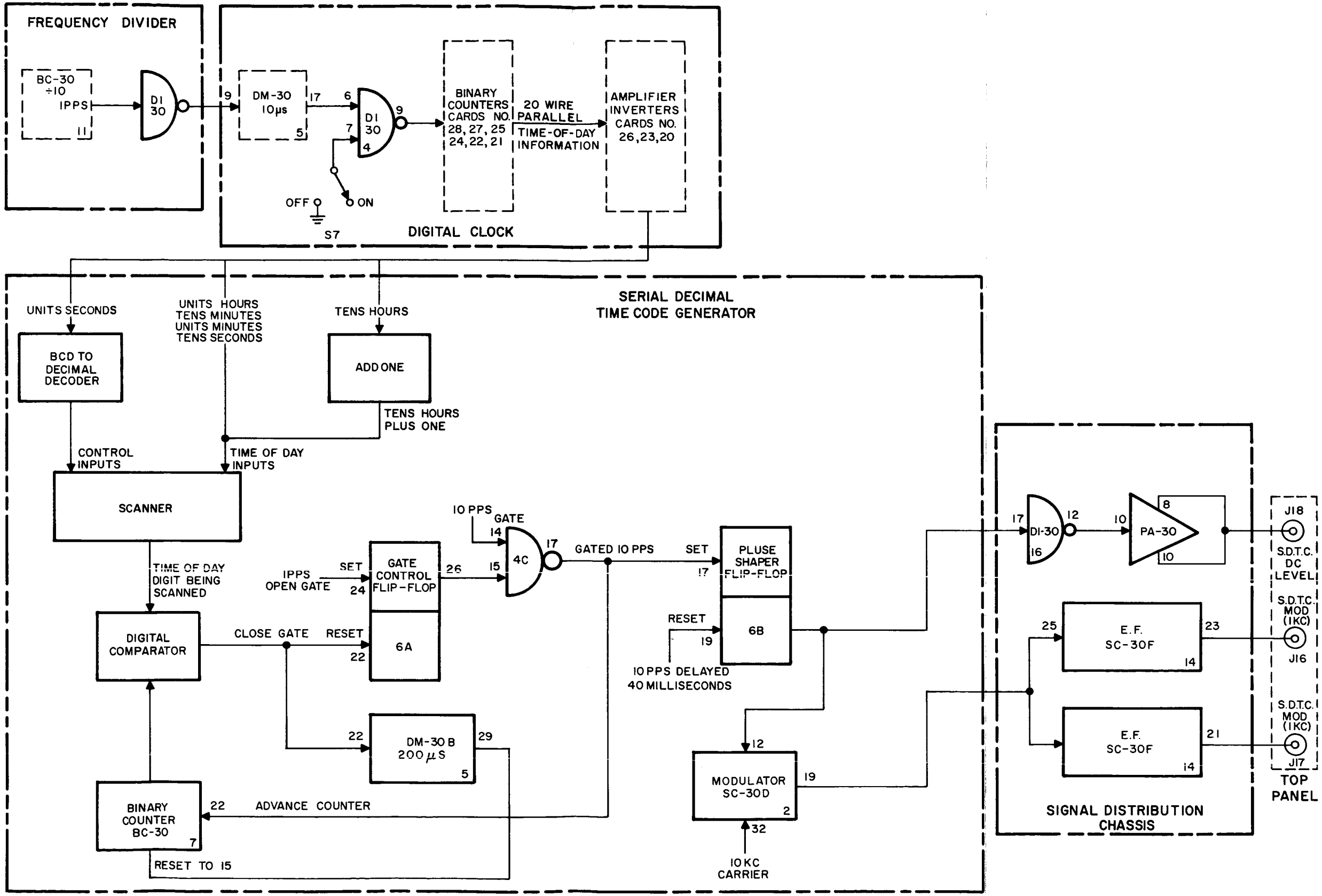


FIGURE 3.32 SERIAL DECIMAL TIME CODE SIGNAL DEVELOPMENT

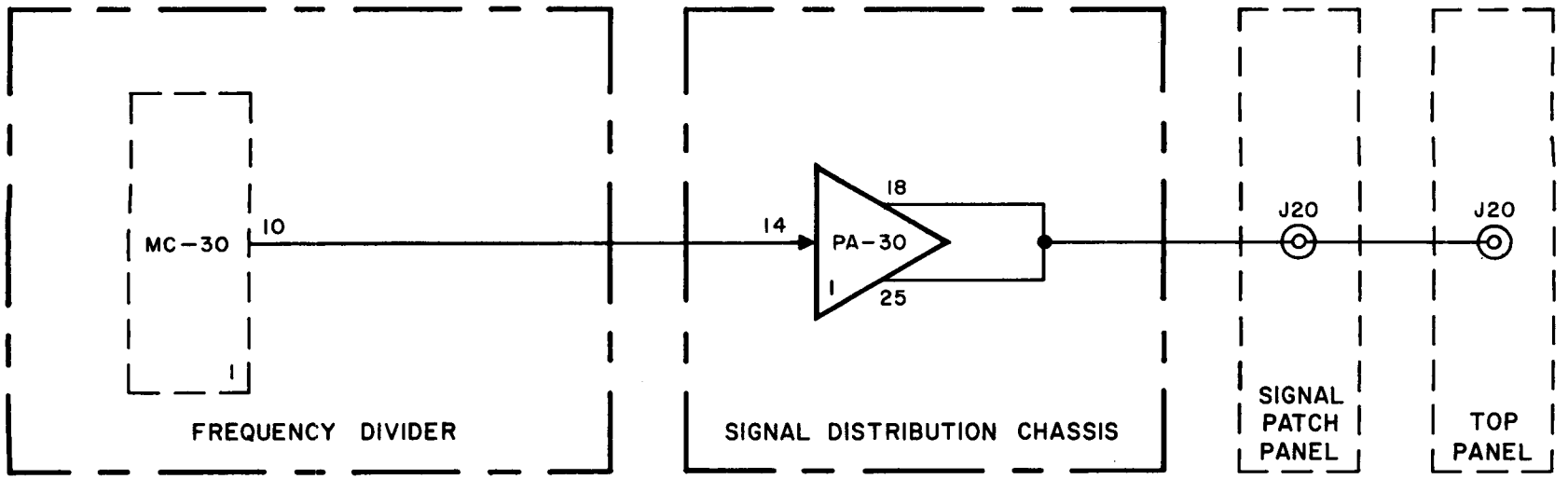


FIGURE 3.33 1-MC 6-4 WAVE SIGNAL DEVELOPMENT

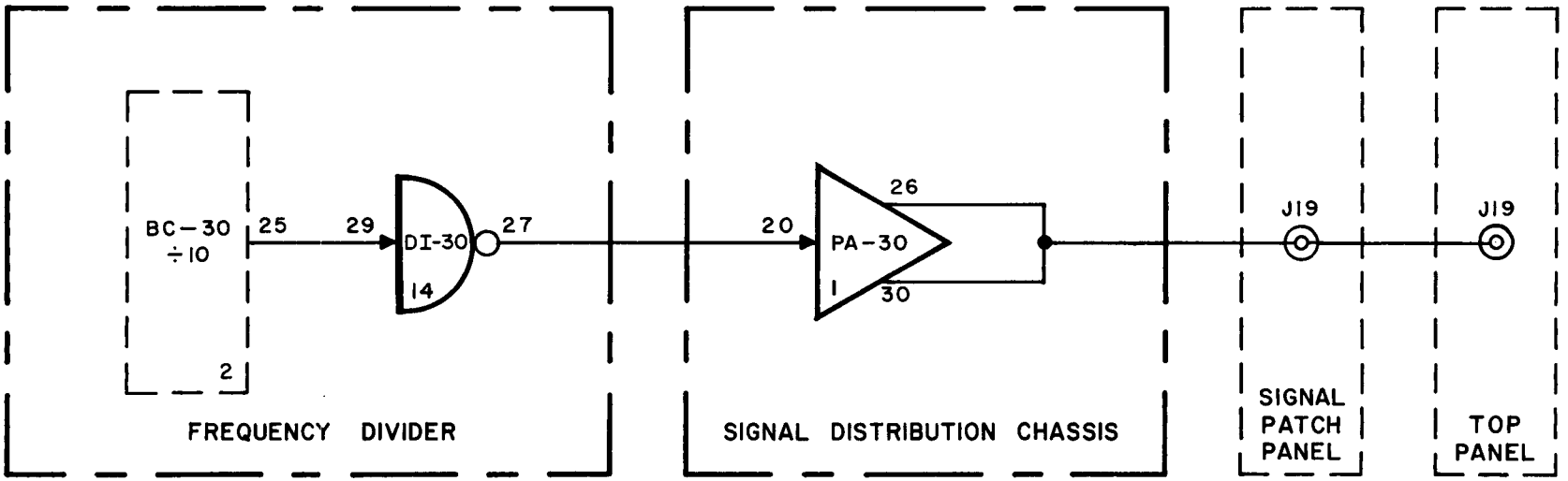


FIGURE 3.34 500,000-PULSE-PER-SECOND SIGNAL DEVELOPMENT

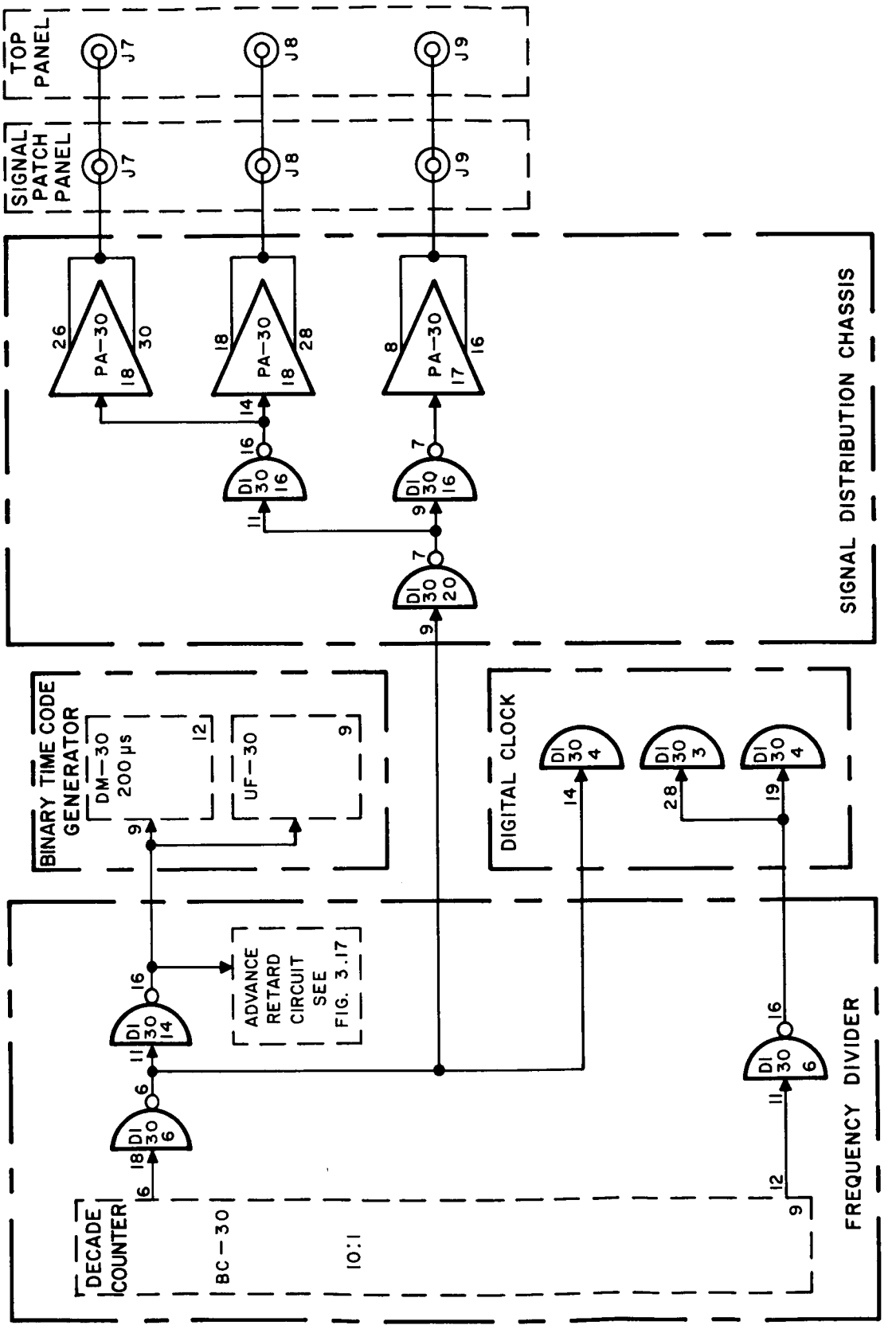


FIGURE 3.35 10-PULSE-PER-SECOND SIGNAL DEVELOPMENT

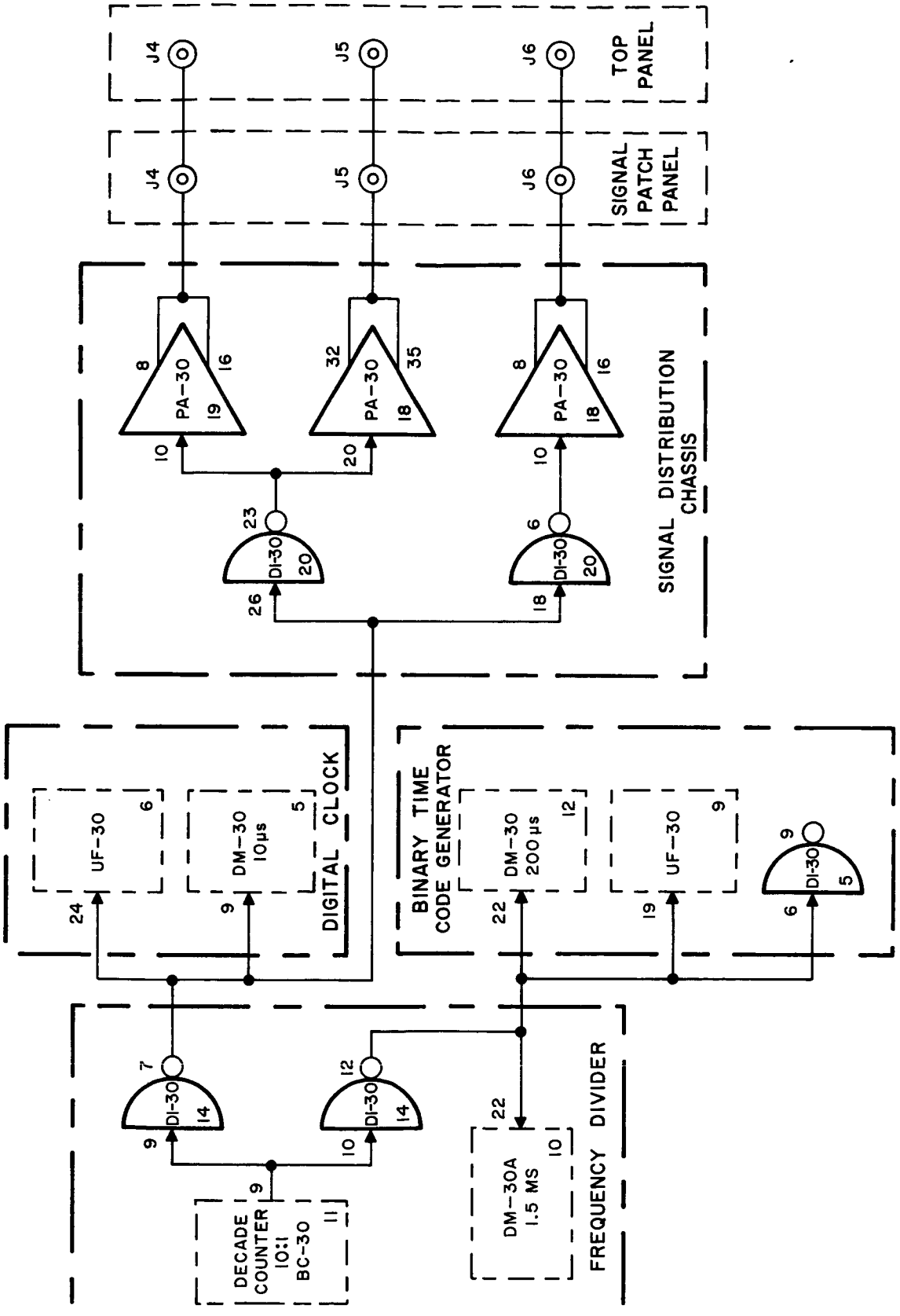


FIGURE 3.36 1-PULSE-PER-SECOND SIGNAL DEVELOPMENT

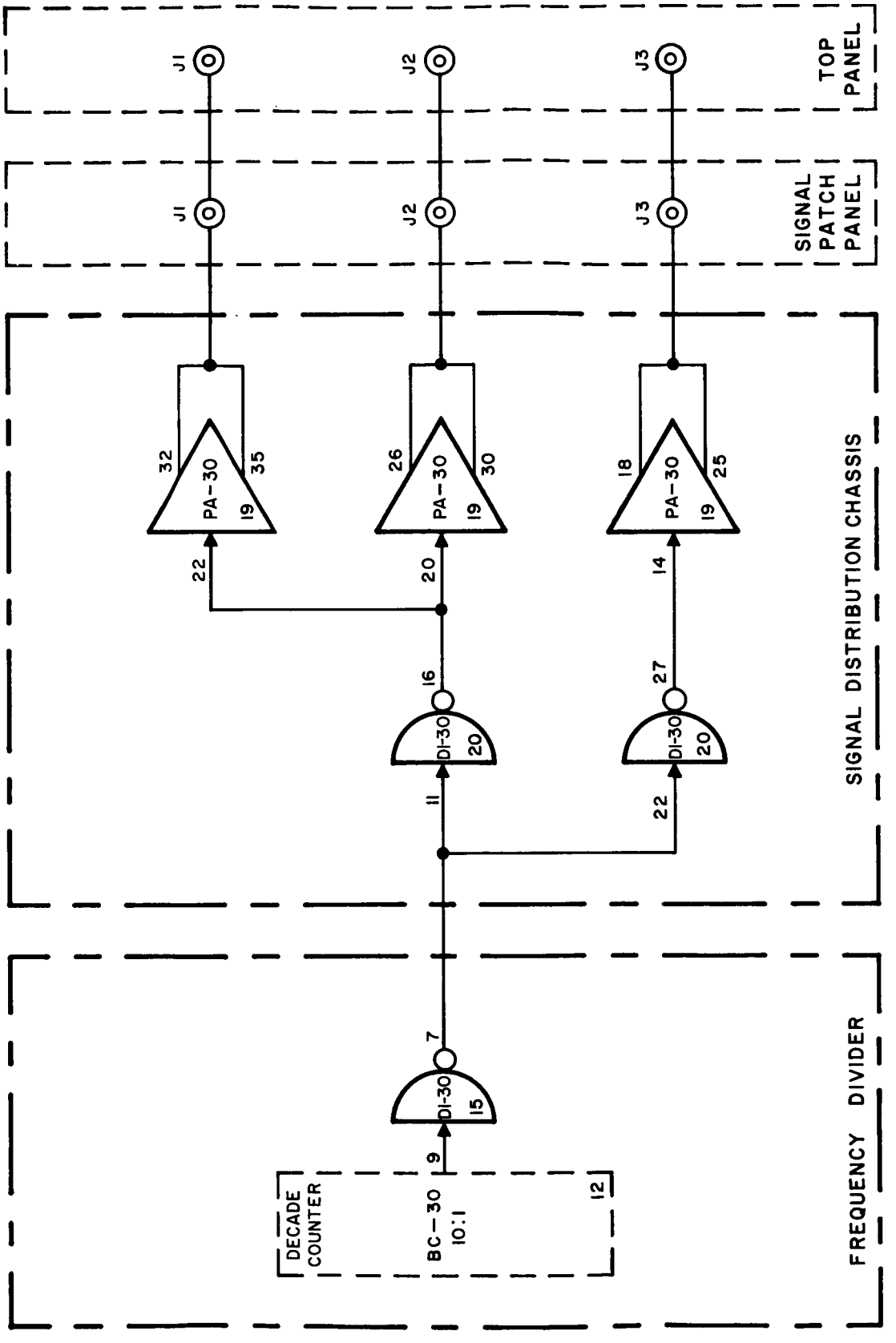


FIGURE 3.37 6-PULSE-PER-MINUTE SIGNAL DEVELOPMENT

SECTION 4
SYSTEM MAINTENANCE

4.1 GENERAL

This section includes information for preventive maintenance, performance testing, analyzing, repairing, and lubrication of the system.

The tables covering system performance tests and unit performance can be used to satisfy performance specifications for a repaired unit or a newly installed time standard rack. The diagrams on trouble analysis will aid maintenance personnel in localizing a malfunction systematically and expeditiously.

The information given in this section will be concerned mainly with the items designed specifically for the Data Acquisition System Timing Standard. Detailed information on the maintenance of commercially manufactured items is available in the manuals published by the manufacturer. Table 1.1 lists such items together with the name of the manufacturer and the titles of the publications involved.

4.2 PREVENTIVE MAINTENANCE

A. General

Most of the preventive maintenance on the timing system must be accomplished with the equipment in operation, since continuous operation is essential for accurate timing signals. With this exception regarding continuous operation, there are few, if any, special preventive maintenance procedures. Some precautions must be observed, however. These precautions are designed mainly to prevent the introduction of inaccuracies into the timing signals while the equipment is in operation.

B. Maintenance Schedule

The maintenance schedule given in Table 4.1 is to be used as a guide until accumulated experience and operational records can provide information for a more realistic schedule.

TABLE 4.1
MINIMUM PREVENTIVE MAINTENANCE SCHEDULE

Schedule	Operation to be accomplished
Daily	Check the site logs for entries which will indicate potential trouble in the equipment
	Check the meters and indicators on the various panels of the time standard rack and observe if they are functioning properly
	Check timing signal with station WWV in accordance with section 2 paragraph 2.3 of this manual
	Observe all the time-indicating equipment which is operated by the time signals from the time standard
	Check the operation of the fans in the WWV receiver, the Tektronic Type 503 oscilloscope, and the fans at the top of each rack. It is not an uncommon occurrence for small fans concealed in the equipment to become inoperative without detection
Weekly	Check the 28-volt battery in accordance with the procedures in paragraph 4.2.c
Monthly	Make a physical inspection of the equipment as outlined in paragraph 4.2.c
	Minimum-performance tests should be made. Table 4.2 lists these tests and the procedures to follow. Personnel conducting these tests on an operational timing system should particularly observe the notes regarding the prevention of timing signal interruption

C. Maintenance Procedures

(1) Detection of abnormal conditions in the equipment by visual or audible means is quite often possible during the physical inspection. During such an inspection, maintenance personnel should be alert for cleanliness of the equipment, lost or missing hardware, abnormal meter readings, and unusual rhythm and noises from moving parts such as fans. All indicator lamps should operate

properly and no wiring or cabling should be under mechanical strain. The prompt correction of all apparent discrepancies, regardless of how minor they may seem, will increase the reliability of the equipment.

(2) It is very important that the nickel-cadmium batteries be maintained in a dependable status. The purpose of an emergency power supply is defeated if attention to these batteries is neglected. There are some general rules of battery maintenance which should be followed. These are given below in condensed form:

(a) Maintain the batteries in a healthy state of charge

(b) Keep the batteries clean

(c) Keep a written record of maintenance performed on the batteries

(3) Rusted or corroded metal surfaces should be cleaned and then refinished by painting with a matching color. In the case of plated metal which is severely scratched, a coat of clear lacquer should be applied.

D. Precautions Taken During Maintenance Operations

(1) Damage may result from operating the time standard equipment without the batteries connected to the emergency power supply. Always make certain the fuse at the rear of the emergency supply is installed before the "AC POWER" switch is turned on. When the time standard equipment is turned off, the fuse may be removed only after the "AC POWER" switch has been turned off. If for any reason it becomes necessary to make a change in the batteries with the time standard rack in operation, make certain that the fresh battery is properly connected to the emergency power supply circuit before disconnecting the old battery.

(2) Careless operation of switches and controls located on the time standard and HP 104 AR ultrastable oscillator will introduce inaccuracies in the time signals which may require a lengthy operation to remove. Momentary operation of these switches will necessitate recalibration and adjustment of the timing equipment to WWV. A lengthy stabilization period may be necessary after any

movement of the setting of the frequency controls on the HP 104 AR oscillator. The above precautions do not preclude making the necessary adjustments when they are obviously needed.

(3) The preventive maintenance checks should be selected with great care to avoid interrupting the timing signals which are in use. Maintenance personnel responsible for making preventive maintenance checks should observe the notes associated with such steps in the tables. In many checks where the signals are measured at a particular jack number it is advisable and more convenient to connect the leads of the test equipment to the wired side of the jack. consult the schematic and logical block diagrams in Section 6 when attempting to locate a test point other than that designated.

4.3 PERFORMANCE STANDARDS

A. General

(1) The steps listed in Table 4.2 are those necessary for checking a complete time standard rack. The specifications listed meet factory standards. Since some of the specifications are dependent upon signals which are furnished by a combination of units, it is necessary to make certain that all units involved are in good operating condition. The steps listed in this table are in order of signal development. For assurance that the time standard rack is checked completely, it is recommended that the checks be performed in proper sequence.

(2) The tests which may be performed for preventive maintenance purposes are marked with an asterisk (*).

TABLE 4-2
PERFORMANCE STANDARD FOR TIME STANDARD RACK

Step	Procedure	Minimum acceptable performance
1. Power check	Check the following controls and indicators: *A. Check that the "AC POWER" switch on the emergency power transfer panel is in the "ON" position.	

TABLE 4.2 - continued
PERFORMANCE STANDARD FOR TIME STANDARD RACK

Step	Procedure	Minimum acceptable performance
1. (continued)	Check that power is applied to: (1) Frequency Divider (2) HP 104 AR Oscillator (3) 60-cps generator-amplifier circuit (4) Panel clock (should be running)	
	*B. Use "VOLTAGE MONITOR" switch located on the emergency power transfer panel and associated dc voltmeter to measure voltage from emergency power supply	The dc voltmeter should read -6VDC, +12VDC, -18VDC, -28VDC, and -30VDC
	Check to make sure fuse at rear of emergency power supply has been installed	
	Turn "AC POWER" switch on emergency power transfer panel to the "OFF" position	
	*C. Repeat B above At completion of C turn "AC POWER" switch to "ON" position	AC power indicating light should light
	*D. Check to make sure "CHARGE RATE" switch is in "NORMAL CHARGE" position	Normal-charge indicating light should be lit; "CHARGE RATE" meter should read 100 ma

TABLE 4.2 - continued
PERFORMANCE STANDARD FOR TIME STANDARD RACK

Step	Procedure	Minimum acceptable performance
1. (continued)	*E. Place "CHARGE RATE" switch in "FAST CHARGE" position	Fast-charge indicator light should light; "CHARGE RATE" meter should read one ampere
	At completion of E above turn "CHARGE RATE" switch back to "NORMAL CHARGE" position	
	*F. Use "VOLTAGE MONITOR" switch located on power control panel and associated dc voltmeter to measure voltages from RP-32 power supply	The dc voltmeter should read: +12 VDC, -6VDC, and -18VDC
	*G. Check time-of-year indicators and seconds indicators	Indicators should all be operating
	*H. Turn "AC POWER" switch on following equipment to "ON" position: (1) WWV Receiver (2) Tektronix oscilloscopes	Power-on indicating light should light
2. One-megacycle oscillator check	*A. Check output level of 1-megacycle oscillator by use of an oscilloscope	NOTE: Oscillator must have been in operation at least 3 hours before normal indications can be expected: 1-mc signal, 1 volt peak to peak

TABLE 4.2 - continued
PERFORMANCE STANDARD FOR TIME STANDARD RACK

Step	Procedure	Minimum acceptable performance
3. 60-cps sine wave check	Check operation of panel clock	
	*A. Connect an oscilloscope across terminals B and C of IT-226A ERA	Signal should be a 60-cps sine wave approximately 105 volts peak to peak
	*B. Connect an external ac meter across the panel clock	Meter should read same as ac meter located on clock amplifier panel
4. Check of one-pulse-per-second signal	NOTE: For preventive maintenance check, when signal is in use, take measurements at top panel	
	*A. Measure one-pulse-per-second signal at J4, J5, or J6 by use of an oscilloscope and observe:	Ground level for 800 ms and at a -6 volts for 200 ms
	*B. Observe 1-second time interval from WWV on time-standard-rack oscilloscope	Coincident condition between signal from WWV and local 1-pulse-per-second signal is obtained. Maximum allowable drift is 1 ms in 24 hours
	*C. Observe seconds display on digital clock while listening to WWV time check from WWV RECEIVER	Seconds indicator advances in exact synchronization with time signal heard from WWV

TABLE 4.3
PERFORMANCE STANDARD FOR FREQUENCY DIVIDER CHASSIS

Step	Procedure		Minimum acceptable performance
1. Divider chain	Use Figure 3.2 and a dual-trace oscilloscope when conducting the following checks:		
	A. Measure the 1-mc signal at pin 18, card 1 (MC-30)		Signal should be a 1-mc sine wave with 1 volt peak to peak
	B. Check frequency dividing action of cards 2 and 3 (BC-30) by connecting oscilloscope as follows:		NOTE: The following division ratios are correct. For the wave shapes see the S-PAC Instruction Manual
	Trace A	Trace B	
	pin no.	pin no.	
	Card 2		
	22	25	2-to-1 frequency division
	22	18	10-to-1 frequency "
	22	6	10-to-1 frequency "
	Card 3		
	22	18	10-to-1 frequency division
	22	12	10-to-1 frequency "
	C. Check operation of phase shifter by placing oscilloscope across terminals S1 and S3 of Reeves R-150 Resolver (see Fig. 3.3)		Signal should be a 10-kc sine wave

TABLE 4.3 - continued

PERFORMANCE STANDARD FOR FREQUENCY DIVIDER CHASSIS

Step	Procedure		Minimum acceptable performance
	Connect oscilloscope to pin 33		Output should be a 10,000-pulse-per-second square wave
	D. Connect oscilloscopes to pin 23, card 6B		Output should normally be a 10,000-pulse-per-second square wave
	E. Check frequency dividing action of cards 7, 8, 9, 11, 12, and 13 (BC-30) by connecting oscilloscope as follows:		
	Trace A pin no.	Trace B pin no.	
	Card 7		
	22	18	10-to-1 frequency division
	22	9	10-to-1 frequency division
	22	6	10-to-1 frequency division
	Card 8		
	22	25	2-to-1 frequency division
	22	9	10-to-1 frequency division
	22	6	10-to-1 frequency division
	Card 9		
	22	12	10-to-1 frequency division
	22	6	10-to-1 frequency division
	Card 11		
	22	25	2-to-1 frequency division
	22	9	10-to-1 frequency division
	22	6	

TABLE 4.3 - continued
PERFORMANCE STANDARD FOR FREQUENCY DIVIDER CHASSIS

Step	Procedure	Minimum acceptable performance
	Card 12	
	22 25	2-to-1 frequency division
	22 33	5-to-1 frequency division
	22 12	10-to-1 frequency division
	22 9	10-to-1 frequency division
	Card 13	
	22 25	2-to-1 frequency division
	22 33	6-to-1 frequency division
	22 9	6-to-1 frequency division
2. Advance-retard circuit	Use Figure 3.4 when conducting the following checks: Connect trace A to pin 25 and trace B to pin 31 of card 5 (DM-30) Set the "RATE-SELECTOR" switch S2 to the following positions:	Signals appearing on oscilloscope should be as follows: Trace A Trace B
	(1) 100 MS/SEC position	1000-PPS 6-4 wave; 10-microsec-wide-pulse at 1,000-PPS rate
	(a) move trace B to pin 33 card 6 (DI-30)	Inverted 10-microsec-wide pulse at 1,000-PPS rate

TABLE 4.3 - continued
PERFORMANCE STANDARD FOR FREQUENCY DIVIDER CHASSIS

Step	Procedure	Minimum acceptable performance
	(b) move trace B to pin 29 card 6 (DM-30)	Trace A: Trace B 10-micro-sec-wide pulse at 1,000-PPS rate
	(c) place the "ADVANCE-RETARD" switch in the "R" position. Move trace B to pin 31 of card 10 (DM-30A)	140-micro-sec-wide pulse at 1,000-PPS rate
	(2) Repeat the above procedure for 10-MS/SEC position and 1-MS/SEC position	In 10-MS/SEC position signal appearing on oscilloscope should be 100 PPS and 1-MS/SEC position signal should be 10 PPS
3. Time comparison circuit	Use Figure 3.5 when conducting the following checks:	
	(1) connect oscilloscopes as follows: Trace A: Pin 25, card 8 (BC-30) Trace B: Pin 9, card 11 (BC-30)	Signals appearing on oscilloscope should be as follows: Trace A: 6-4 500 PPS Trace B: 6-4 1PPS
	(2) Remove trace B and connect it to pin 12 of card 14 (DI-30)	Signal should be an inverted 1-PPS signal
	(3) Remove trace B and connect it to pin 10 of card 10(DM-30A)	Signal should be a 1.5-ms-wide pulse, at a repetition rate of 1 PPS

TABLE 4.3 - continued

PERFORMANCE STANDARD FOR FREQUENCY DIVIDER CHASSIS

Step	Procedure	Minimum acceptable performance
	(4) Remove trace B and connect it to pin 23 of card 14 (DI-30)	Signal should be a 1-ms-wide pulse at a repetition rate of 1 PPS
	(5) Remove trace A and connect it to pin 19 of card 16 (SC-30B)	Signal appearing on trace A should be a 1-ms-wide puise delayed by 1 MS from signal appearing on trace B
	(6) Connect output from WWV receiver to pin 25 card 16 (SC-30B)	Signal appearing on trace A should be the WWV time tick with delayed 1-MS-wide pulse occurring at positive zero crossing of second cycle
4. 60-cps generator and synchronized inverter	Use Figure 3.6 when conducting the following checks:	
	(1) Connect trace A to pin 12 of card 8 (BC-30) and trace B to pin 9 of card 17 (ST-30)	Signal appearing on trace A will be 100 PPS and signal appearing on trace B will be 600 CPS
	(2) Move trace B to pin 10 of card 17 (ST-30)	Signal appearing on trace will be 600 PPS
	(3) Move trace A to pin 20 of card 18 (BC-30)	Signal appearing on trace will be 60 PPS, resulting in a 10 to 1 frequency division
	(4) Connect oscilloscope across pin 3 and 6 of IT-226A ERA DC-AC inverter	Signal will be 105 volts peak to peak for a 60-cps sine wave

TABLE 4.4
PERFORMANCE STANDARD FOR DIGITAL CLOCK CHASSIS

Step	Procedure	Minimum acceptable performance
	Use Figures 6.4 and 3.8 and a dual-trace oscilloscope when conducting the following checks:	
	A. Connect trace A to pin 9 and trace B to pin 17 of card 5 (DM-30)	Signal appearing on trace A will be a 1-PPS signal and the signal appearing on trace B will be a negative-going 10-microsecond-wide pulse occurring once each second
	B. Remove trace A and connect it to pin 9 of card 4	The signal appearing on the oscilloscope will be a positive-going 10-microsecond-wide pulse occurring once each second
	Use Figures 6.4 and 3.8 when conducting the following checks: C. Check frequency-dividing action of the decade counters as follows:	
	Card 22 22 25 22 33 22 12 22 9 22 6	 2-to-1 frequency division 5-to-1 frequency division 10-to-1 frequency division 10-to-1 frequency division 10-to-1 frequency division
	Card 21 22 25 22 33 22 6	 2-to-1 frequency division 10-to-1 frequency division

TABLE 4.4 - continued
PERFORMANCE STANDARD FOR DIGITAL CLOCK CHASSIS

Step	Procedure		Minimum acceptable performance
	Card 19		
	22	25	2-to-1 frequency division
	22	33	5-to-1 frequency division
	22	12	10-to-1 frequency division
	22	9	10-to-1 frequency division
	22	6	10-to-1 frequency division
	Card 18		
	22	25	2-to-1 frequency division
	22	33	5-to-1 frequency division
	22	12	10-to-1 frequency division
	22	9	10-to-1 frequency division
	22	6	10-to-1 frequency division
	Trace A pin no.	Trace B pin no.	
	Card 28		
	22	25	2-to-1 frequency division
	22	33	5-to-1 frequency division
	22	12	10-to-1 frequency division
	22	9	10-to-1 frequency division
	22	6	10-to-1 frequency division
	Card 27		
	22	25	2-to-1 frequency division
	22	33	5-to-1 frequency division
	22	9	10-to-1 frequency division
	22	6	10-to-1 frequency division
	Card 25		
	22	25	2-to-1 frequency division
	22	33	5-to-1 frequency division
	22	12	10-to-1 frequency division
	22	9	10-to-1 frequency division

TABLE 4.4 - continued
PERFORMANCE STANDARD FOR DIGITAL CLOCK CHASSIS

Step	Procedure		Minimum acceptance performance
	Card 24		
	22	25	2-to-1 frequency division
	22	33	6-to-1 frequency division
	22	9	6-to-1 frequency division
	22	6	6-to-1 frequency division
	Card 17		
	22	25	2-to-1 frequency division
	22	33	
	Compare the seconds displayed on the display panel with the seconds displayed on the clock amplifier panel		The two displays should be the same and should change in unison
	Use Figure 6.4 and 3.8 and a dual-trace oscilloscope when conducting the following checks:		
	A. Connect trace A in order shown below		Use Figure 3.8 when conducting this check; numb ers shown below correspond to trace numbers on figure
	Pin	Card	Trace no.
	33	9	3
	23	9	4
	23	11	5
	16	11	6
	7	11	7
	24	6	8
	6	26	9
	14	4	10
	17	4	11
	28	3	12
	27	8	13
	29	5	14

TABLE 4.5

PERFORMANCE STANDARD FOR SERIAL DECIMAL TIME CODE GENERATOR

Procedure: Use Figures 6.6 and 3.8 and a dual-trace oscilloscope when conducting the following checks. Trace numbers correspond to trace numbers shown in Figure 3.8.

A. Connect trace A in order shown below:

Pin	Card	Trace No.
33	9	3
23	9	4
23	11	5
16	11	6
7	11	7
24	6	8
6	26	9
14	4	10
17	4	11
28	3	12
27	8	13
29	5	14
21	4	15
6	6	6 (SDTC output)

TABLE 4.6
PERFORMANCE STANDARD FOR THE BINARY TIME CODE GENERATOR

Step	Procedure	Minimum acceptable performance
1. Clear and read in Pulse Generator	Use Figures 3.14 and 3.15 and a dual-trace oscilloscope when conducting the following checks:	
	A. Connect trace A to pin 22 and trace B to pin 29 of card 12 (DM-30)	The signal appearing on trace A should be a 1-PPS signal and the signal appearing on trace B should be a 200-microsecond signal occurring once each second
	B. Disconnect trace A and reconnect it first to pin 23 then to pin 27 of card 13 (D1-30)	The signal appearing on the trace should be a 200-microsecond-wide pulse inverted from the signal appearing on trace B in step A
	C. Disconnect trace B and reconnect it to pin 6 of card 12 (DM-30)	The signal appearing on the trace should be a 200-microsecond-wide negative-going pulse delayed 200 microseconds
	D. Disconnect trace A and reconnect it to pin 7 of card 13 (D1-30)	The signal appearing on the trace should be a 200-microsecond-wide pulse inverted from the signal appearing on trace B

TABLE 4.6 - continued
PERFORMANCE STANDARD FOR THE BINARY TIME CODE GENERATOR

Step	Procedure	Minimum acceptable performance
	E. Disconnect trace A and reconnect it first to pin 32 and then to pin 26 of card 14(DN-30)	The signal appearing on the trace should be a 200-microsecond-wide positive-going pulse occurring once each second
	F. Disconnect trace B and reconnect it first to pin 8 and then to pin 18 of card 14 (DN-30)	The signal appearing on the trace should be a 200-microsecond-wide negative-going pulse delayed 200 microseconds from the signal appearing on trace A
2. Frame Marker Generator	Use Figure 3.16 when conducting the following checks:	
	A. Connect trace A to pin 6 and trace B to pin 26 of card 5(DN-30)	The signal appearing on trace A should be a 1-PPS signal and the signal appearing on trace B should be a 5-PPS signal
	B. Remove trace B and reconnect it to pin 7 of card 5 (DN-30)	The signal appearing on trace B should be a 10-PPS signal
	C. Remove trace A and reconnect it to pin 9 of card 5 (DN-30)	The signal appearing on the trace should be a 50-millisecond-wide positive-going pulse

TABLE 4.6 - continued
PERFORMANCE STANDARD FOR THE BINARY TIME CODE GENERATOR

Step	Procedure	Minimum acceptable performance
3. Shift pulse generator	Use Figure 3.17 when conducting the following checks:	
	A. Connect Trace A to pin 34 of card 11 (BC-30 and trace B to pin 9 of card 12 (DM-30)	The signal appearing on trace A should be a 100-PPS signal and the signal appearing on trace B should be a 10-PPS signal
	B. Remove trace A and reconnect it to pin 28 of card 12 (DM-30)	The signal appearing on trace A should be a 200-microsecond-wide 10-PPS signal
	C. Remove trace A and trace B. Connect trace A to pin 22 and trace B to pin 6 Card 4 (BC-30)	The signal appearing on trace A should be 1000-PPS signal The signal appearing on trace A should be 1000-PPS signal and the signal appearing on trace B should be a 100-PPS signal. A 10-to-1 frequency division.
	D. Remove trace A and trace B. Connect trace A to pin 18 and trace B to pin 25 of card 11 (BC-30)	The signal appearing on trace A will be a 20-millisecond-wide negative-going pulse occurring every 50 milliseconds

TABLE 4.6 - continued
PERFORMANCE STANDARD FOR THE BINARY TIME CODE GENERATOR

Step	Procedure	Minimum acceptable performance
	E. Remove trace B and connect it to pin 34 of card 13 (DI-30)	The signal appearing on the trace should be a 20-millisecond-wide positive-going pulse occurring once every 80 milliseconds
	F. Remove trace B and connect it to pin 28 of card 8 (DM-30)	The signal appearing on the trace will be a 200-microsecond-wide negative-going pulse appearing once every 100 milliseconds
	G. Remove trace A and connect it to pin 26	The signal appearing on the trace will be a 30-millisecond-wide negative-going pulse occurring once every 70 milliseconds
	H. Remove trace A and connect it to pin 23 of card 6 (DI-30)	The signal appearing on the trace should be a group of four positive-going pulses. (See the waveform at the bottom of Figure 3.17)
	I. Remove trace B and connect it first to pin 6, then to pin 12 and then to pin 16 of card 6 (DI-30)	The signal appearing on the trace at these pins should be the inverted version of the signal appearing on trace A (Step H)

TABLE 4.6 - continued
PERFORMANCE STANDARD FOR THE BINARY TIME CODE GENERATOR

Step	Procedure	Minimum acceptable performance
	J. Remove trace A and connect it in order to the following pins of card 7 (PA-30): 28, 30, 18, 25, 8, and 16	The signal appearing on the trace should be the inverted version of the signal appearing on trace B. (See the last waveforms at the bottom of Figure 3.17)
4. Index marker generator	Use Figures 3.14 and 3.18 when conducting the following checks	
	A. Connect trace A to pin 22 of card 9 (UF-30) and trace B to pin 34 of card 11 (BC-30)	The signal appearing on trace A should be a 10-PPS signal (see the first waveform at the bottom of Figure 3.18) and the signal appearing on trace B should be a 100-PPS signal
	B. Remove traces A and B. Connect trace A to pin 9 and trace B to pin 28 of card 12 (DM-30)	The signal appearing on trace A will be a 10-PPS signal and the signal appearing on trace B will be a 200-microsecond-wide pulse
	C. Remove traces A and B. Connect trace A to pin 33 and trace B to pin 27 of card 11 (BC-30)	The signal appearing on trace A should be like the second trace and the signal appearing on trace B should be like the fifth trace shown at the bottom of Figure 3.18

TABLE 4.6 - continued
PERFORMANCE STANDARD FOR THE BINARY TIME CODE GENERATOR

Step	Procedure	Minimum acceptable performance
	D. Remove traces A and B. Connect trace A to pin 35 and trace B to pin 15 of card 9 (UF-30)	The signal appearing on trace A should be like the third trace and the signal appearing on trace B should be like the sixth trace shown at the bottom of Figure 3.18
	E. Remove traces A and B. Connect trace A to pin 13 of card 5 (DN-30)	The signal appearing on the trace should be like the last trace shown at the bottom of Figure 3.18
5. Read Gate Generator	Use Figure 3.19 when conducting the following checks	
	A. Connect trace A to pin 25 and trace B to pin 27 of card 11 (BC-30)	The signal appearing on trace A should be like the first trace and the signal appearing on trace B should be like the second trace shown at the bottom of Figure 3.19
	B. Remove traces A and B. Connect trace A to pin 17 and trace B to pin 15 of card 10 (UF-30)	The signal appearing on trace A should be like the third trace and the signal appearing on trace B should be like the fourth trace shown at the bottom of Figure 3.19

TABLE 4.6 - continued
PERFORMANCE STANDARD FOR THE BINARY TIME CODE GENERATOR

Step	Procedure	Minimum acceptable performance
	Connect trace A to pin 12 and trace B to pin 19 of card 2 (SC-30E)	The signal appearing on trace A should be the NASA 1/Sec BTC DC Level Shift time code and the signal appearing on trace B should be the modulated NASA 1/Sec BTC (see Figure 3.21 for an example of the BTC format)
	Set the "BLANK" zeros switch located on the control panel to the "BLANK" position. The "ZEROS ARE BLANKED" light should light	

SECTION 5 - PARTS LIST

5.1 GENERAL

This section contains the list of replaceable parts for all of the units in the time standard rack. These lists are made up at the unit level for purchased items. For information on the replacement of components in these purchased items, consult the manufacturers' manuals referenced in Table 1-1.

TABLE 5.1 SPARE PARTS LIST

Item No.	Part Name and Description	Manufacturer	Part No.	Quantity
1	Counter Pac	Computer Control Co., Inc.	BC-30	2
2	Diode Pac		DC-30	1
3	NAND Pac		DI-30	3
4	Delay Multi-vibrator Pac		DM-30	1
5	Adjustable Delay Multi-vibrator Pac		DM-30A	1
6	NAND Pac		DN-30	1
7	Master Clock Pac		MC-30	1
8	Power Amplifier Pac		PA-30	1
9	Shift Register Pac		SR-30	1
10	Schmitt Trigger Pac		ST-30	1
11	Universal Flip-Flop		UF-30	1
12	Phase Shifter Card	NASA Time Measurement Section, GSFC	SC-30A	1
13	600-CPS OSC, Time Comparison, Sync. Transformer Driver		SC-30B	1

TABLE 5.1 SPARE PARTS LIST

Item No.	Part Name and Description	Manufacturer	Part No.	Quantity
1	Counter pac	Computer Control Co., Inc.	BC-30	2
2	Diode pac		DC-30	1
3	NAND pac		DI-30	3
4	Delay multi-vibrator pac		DM-30	1
5	Adjustable delay multivibrator pac		DM-30A	1
6	NAND pac		DN-30	1
7	Master clock pac		MC-30	1
8	Power amplifier pac		PA-30	1
9	Shift register pac		SR-30	1
10	Schmitt trigger pac		ST-30	1
11	Universal flip-flop		UF-30	1
12	Phase shifter card	NASA Time Measurement Section, GSFC	SC-30A	1
13	600-CPS OSC, time comparis-on, Sync. transformer drive		SC-30B	1
14	1-MC cable driver		SC-30C	1

TABLE 5.1 SPARE PARTS LIST

Item No.	Part Name and Description	Manufacturer	Part No.	Quantity
15	Modular card, 10 kc SDTC		SC-30D	1
16	Modular card, 1 kc BTC		SC-30E	1
17	Line drive		SC-30G	1
18	Spare parts kit	Computer Control Co., Inc.	SPK30-7	1
19	Inverter	Sorenson & Co., Inc.	QC28/50/05	1
20	Inverter	Electronic Research Associates, Inc.	IT-226A	1
21	Nixie decoder display	Transistor Electronics Corp.	Model TND-B-A1-BCD	2
22	Rheostat, 60-ohm, 1-w			1
23	Rheostat, 6-ohm, 12.5 watt			1
24	Rheostat, 7.5-ohm, 100-w			1
25	Transistor		2N331	14
26	Transistor		2N404	2
27	Transistor		2N1137A	2
28	Transistor		2N1183	2
29	Transistor		2N1310	2

TABLE 5.1 SPARE PARTS LIST

Item No.	Part Name and Description	Manufacturer	Part No.	Quantity
30	Transistor		2N1313	2
31	Transistor		2N1637 or 2N544	2
32	Zenier diodes, 6-8 v	Motorola, Inc.	1N3016B	4
33	Zenier diodes, 6-8 v	Motorola, Inc.	1/4 M 3.0 AZ5	1
34	Diode		IN1342RA	4
35	Diode		IN270	1
36	Tube		5Y3GT	2
37	Tube		6AN8	2
38	Tube		6AS6	2
39	Tube		6AQ5	2
40	Tube		6BA6	2
41	Tube		6BC6	2
42	Tube		6BC7	1
43	Tube		6BL8/EC-80	2
44	Tube		6DJ8	2
45	Tube		6DQ5	2
46	Tube		6J6/5964	2
47	Tube			
48	Tube		12AU7	2

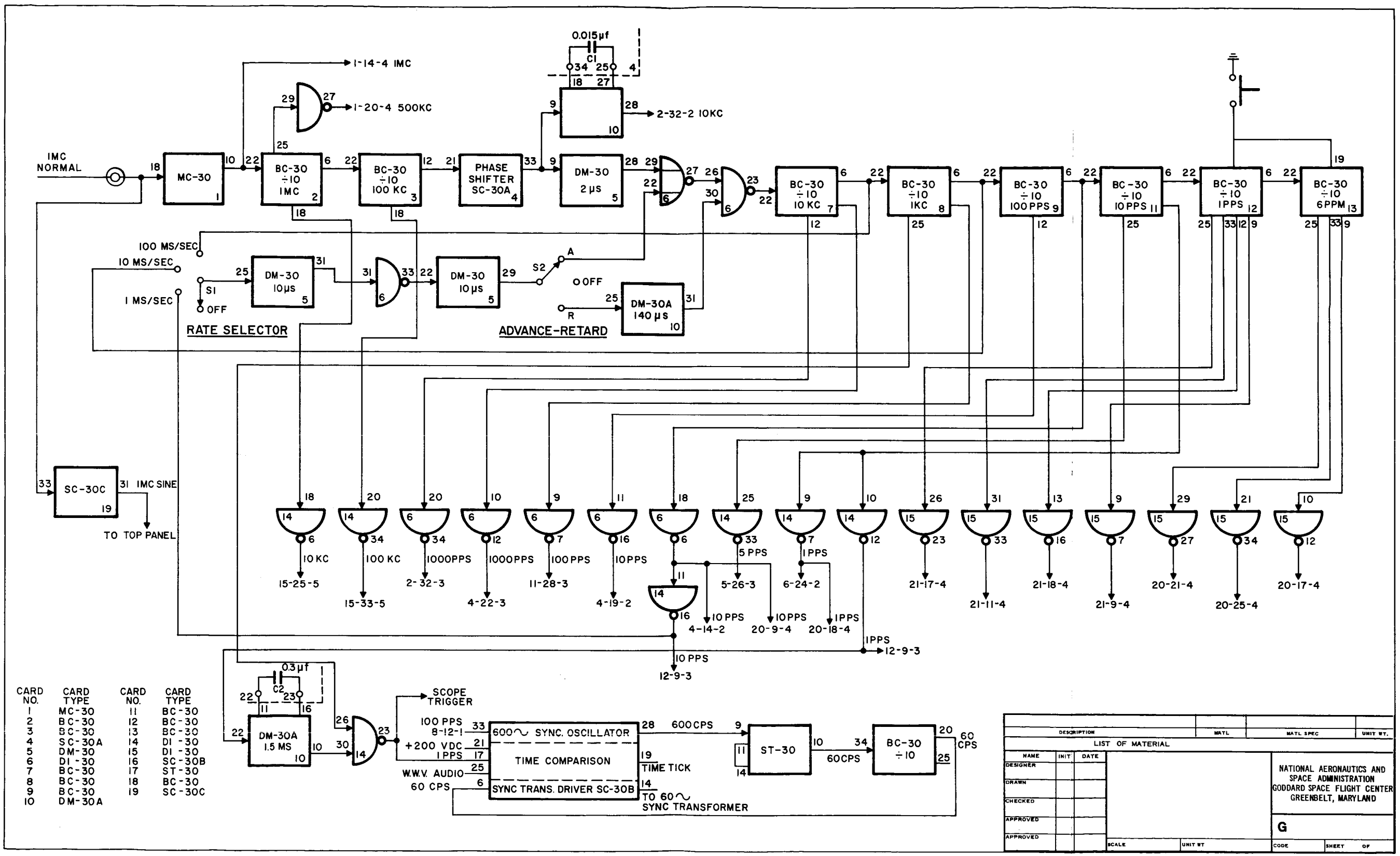
TABLE 5.1 SPARE PARTS LIST

Item No.	Part Name and Description	Manufacturer	Part No.	Quantity
49	Tube		12AT7	2
50	Tube		5642	1
51	Tube		5651	1
52	Fuse, 5-amp., fast		3AG	3
53	Fuse, 3-amp., Slo-Blo		3AG	3
54	Fuse, 1.25-amp., Slo-Blo		3AG	2
55	Incandescent bulb		47	2
56	Spare parts kit	Computer Control Co., Inc.	RP-32 power supply	1

SECTION 6 - SYSTEM DRAWINGS

6.1 GENERAL

This section contains the logical block diagrams of the four units that comprise the time standard and the schematic diagrams of the special circuit cards contained in each unit (Figs. 6.1 to 6.11). For similar information on the purchased items refer to the appropriate manufacturer's instruction manual referenced in Table 1-1.



CARD NO.	CARD TYPE	CARD NO.	CARD TYPE
1	MC-30	11	BC-30
2	BC-30	12	BC-30
3	BC-30	13	BC-30
4	SC-30A	14	DI-30
5	DM-30	15	DI-30
6	DI-30	16	SC-30B
7	BC-30	17	ST-30
8	BC-30	18	BC-30
9	BC-30	19	SC-30C
10	DM-30A		

DESCRIPTION		MATL	MATL SPEC	UNIT WT.
LIST OF MATERIAL				

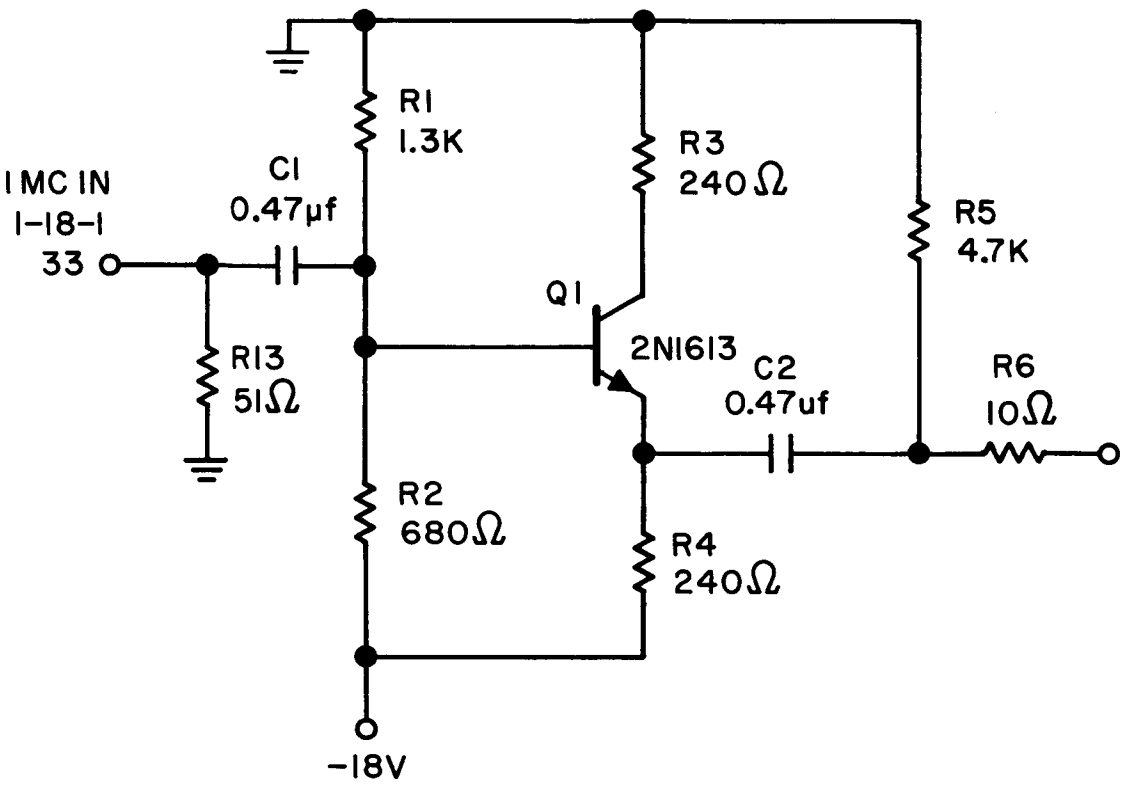
NAME	INIT	DATE
DESIGNER		
DRAWN		
CHECKED		
APPROVED		
APPROVED		

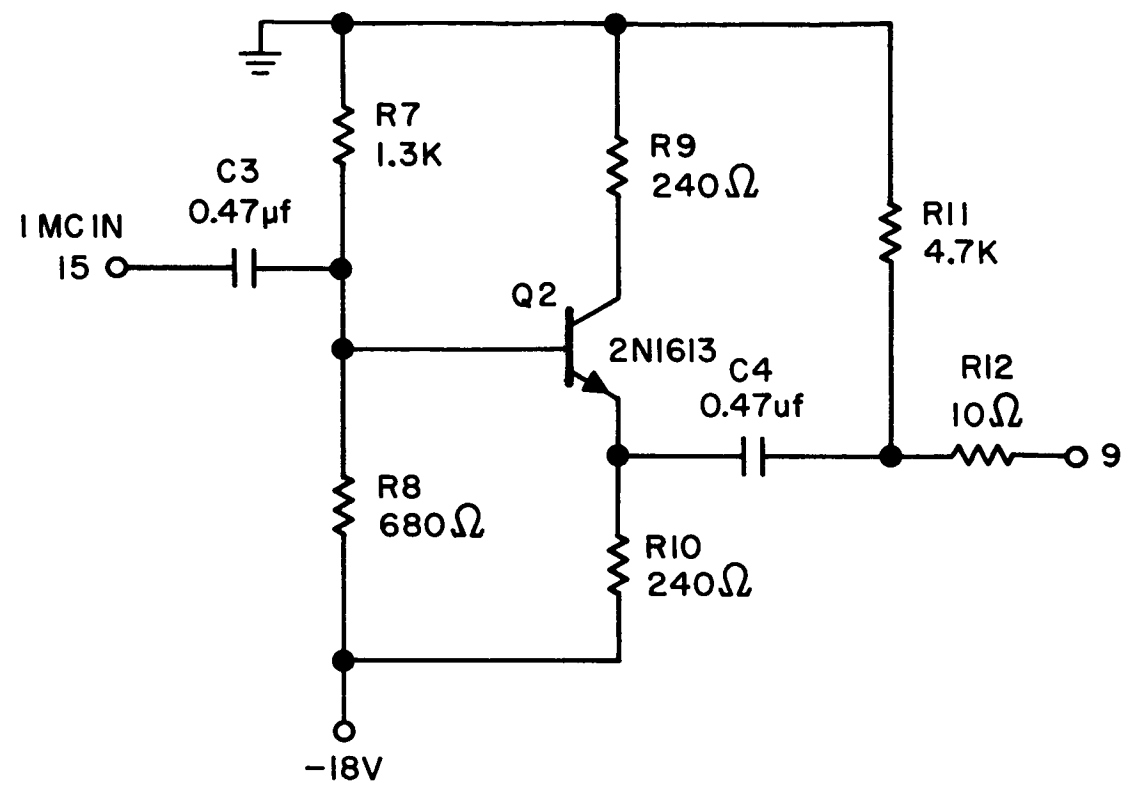
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

G

SCALE | UNIT WT | CODE | SHEET OF

FIGURE 6.1 FREQUENCY DIVIDER, FUNCTIONAL BLOCK DIAGRAM





SIGNATURES		DATE
DESIGNED		
DRAWN		
APPROVED		
DIVISION—		
BRANCH—		
BLDG. / ROOM / PHONE		
SECURITY CLASSIFICATION		

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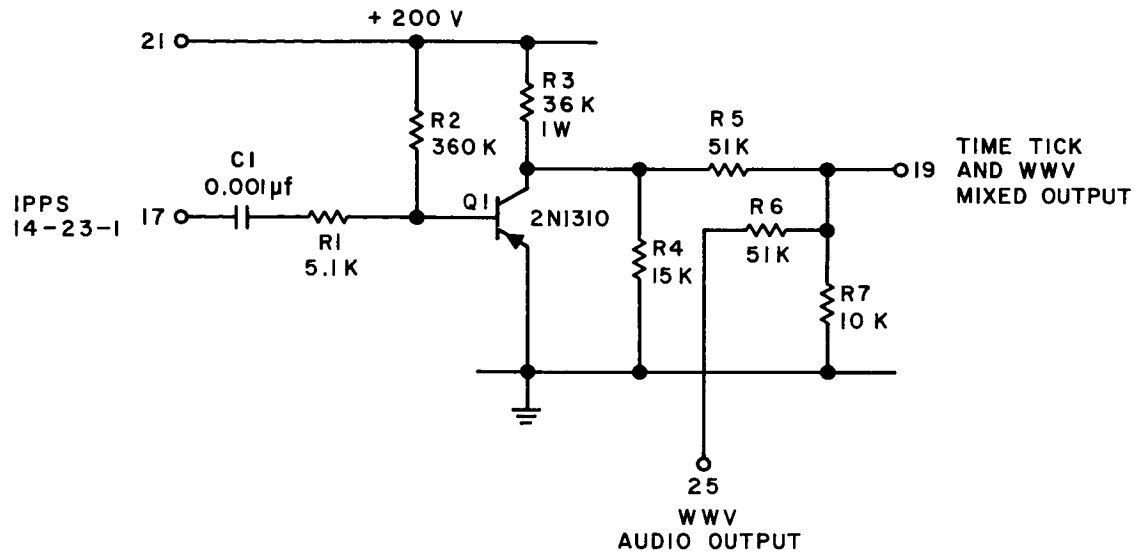
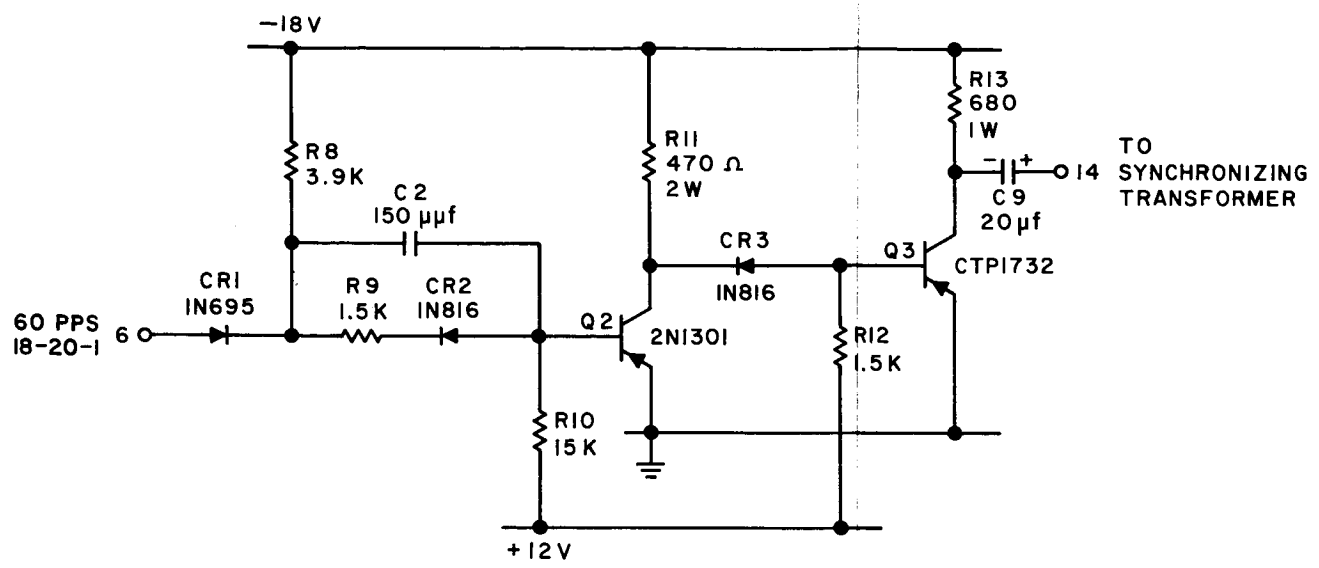
1 MC CABLE DRIVER SC-30C

ASSEMBLY DRAWING NO.	SCALE	DRAWING NO.

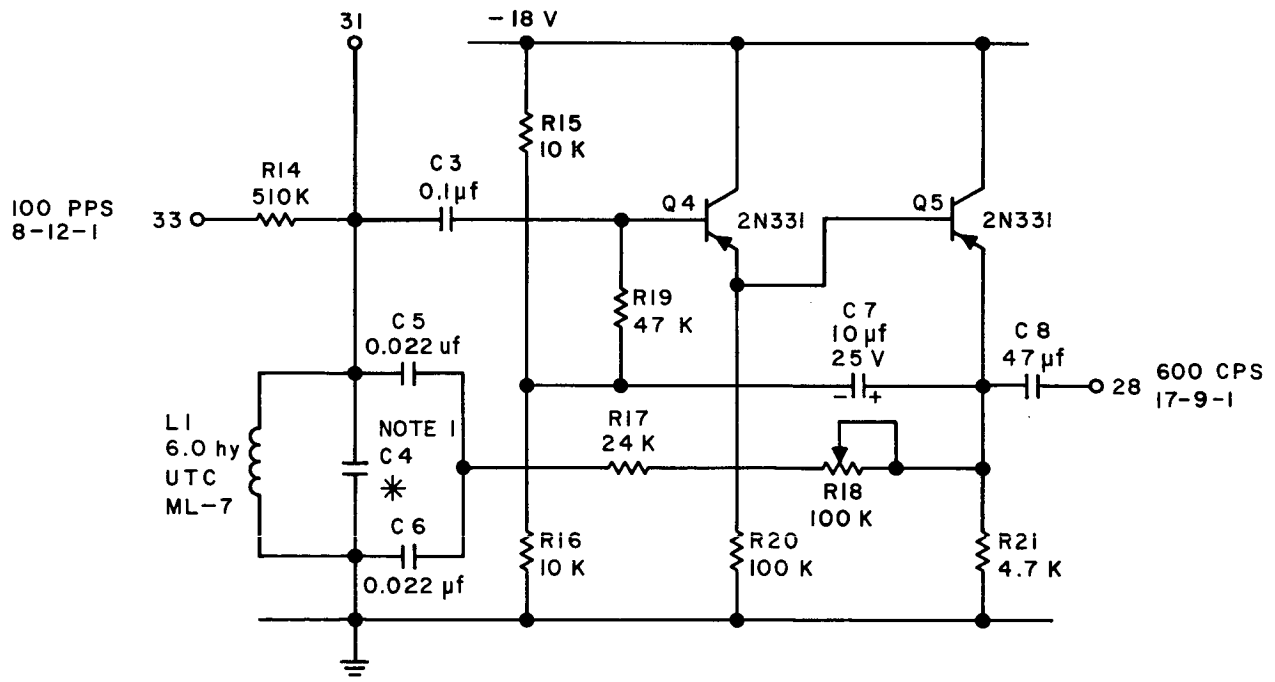
FIGURE 6.2 1-MC CABLE DRIVER (SC-30C)



TIME COMPARISON CIRCUIT



SYNCHRONIZING TRANSFORMER DRIVER



600 CPS SYNCHRONIZED OSCILLATOR

NOTE:

✳ 1. SELECT C4 TO RESONATE TANK AT 600 CPS
2. ADJUST R18 FOR 4 VPP SIGNAL

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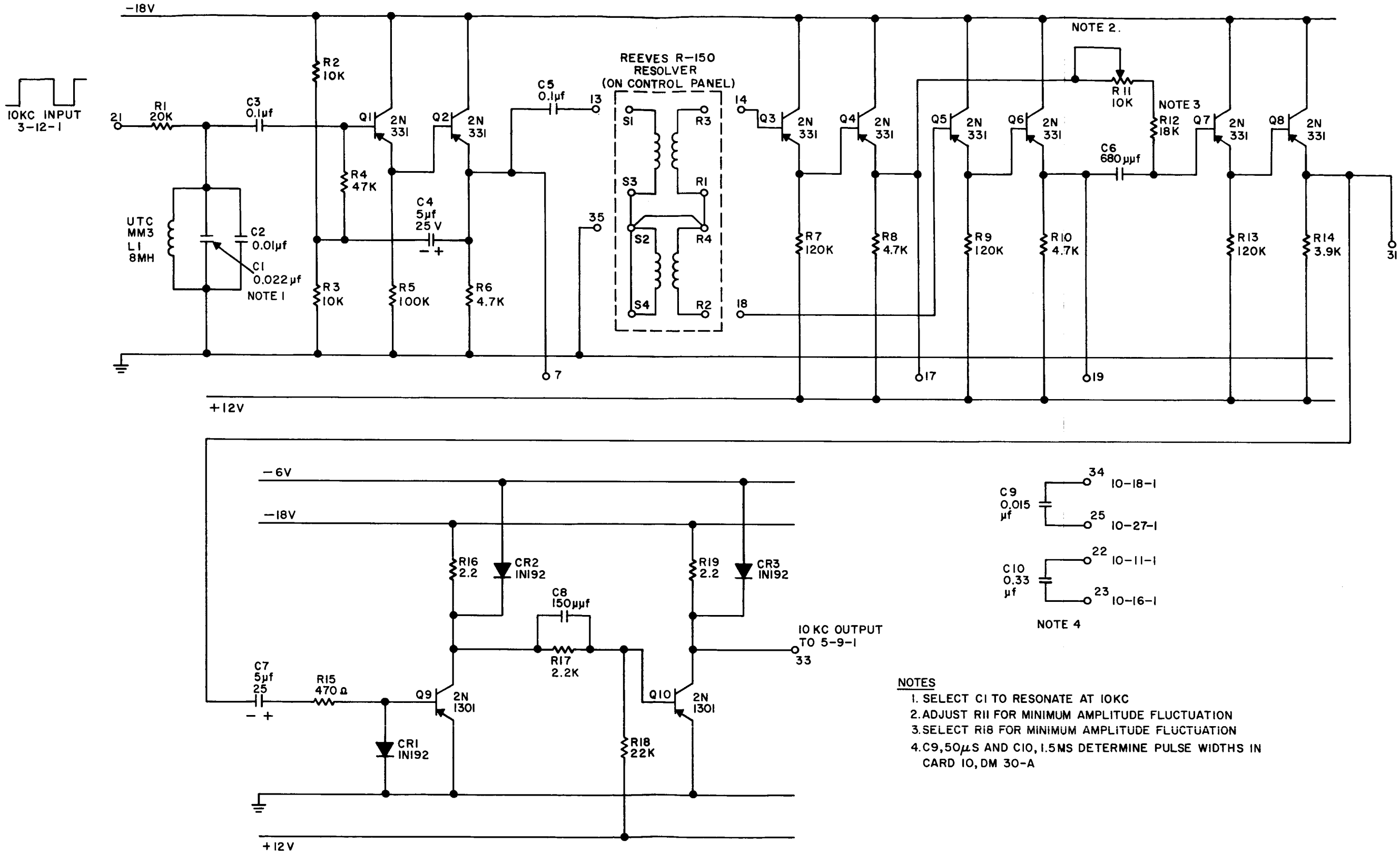
BLDG.	ROOM	PHONE			
SECURITY CLASSIFICATION			ASSEMBLY DRAWING NO.	SCALE	DRAWING NO.

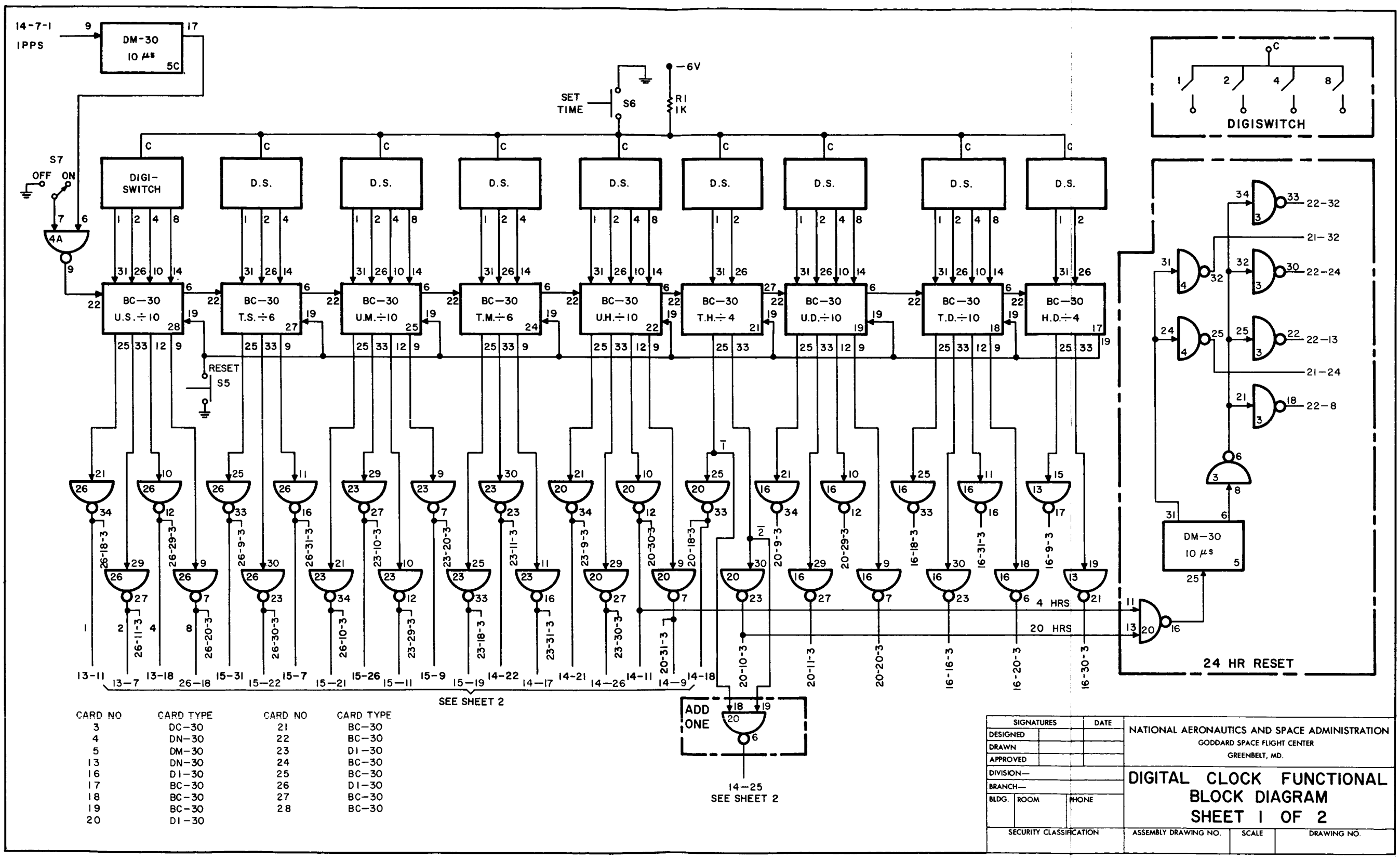
FIGURE 6.3 SPECIAL CIRCUIT CARD (SC-30E)



NOTES

1. SELECT C1 TO RESONATE AT 10KC
2. ADJUST R11 FOR MINIMUM AMPLITUDE FLUCTUATION
3. SELECT R18 FOR MINIMUM AMPLITUDE FLUCTUATION
4. C9, 50μS AND C10, 1.5MS DETERMINE PULSE WIDTHS IN CARD 10, DM 30-A

FIGURE 6.4 PHASE SHIFTER CIRCUIT



CARD NO	CARD TYPE	CARD NO	CARD TYPE
3	DC-30	21	BC-30
4	DN-30	22	BC-30
5	DM-30	23	DI-30
13	DN-30	24	BC-30
16	DI-30	25	BC-30
17	BC-30	26	DI-30
18	BC-30	27	BC-30
19	BC-30	28	BC-30
20	DI-30		

SIGNATURES		DATE
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DIVISION—		
BRANCH—		
BLDG.	ROOM	PHONE

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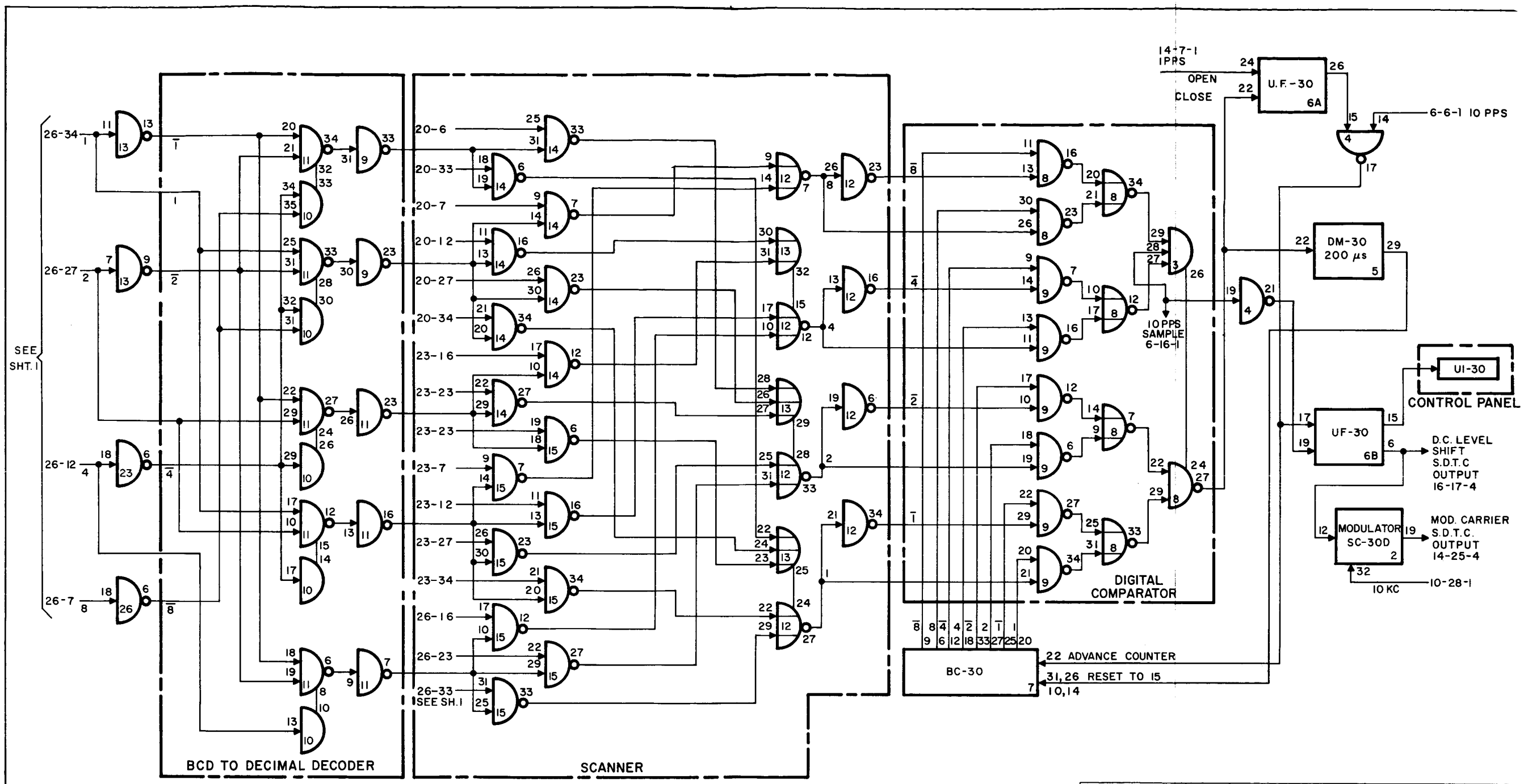
DIGITAL CLOCK FUNCTIONAL BLOCK DIAGRAM
SHEET 1 OF 2

SECURITY CLASSIFICATION	ASSEMBLY DRAWING NO.	SCALE	DRAWING NO.

FIGURE 6.5 DIGITAL CLOCK, FUNCTIONAL BLOCK DIAGRAM
SHEET 1 of 2



CARD NO.	CARD TYPE	CARD NO.	CARD TYPE
2	SC-30D	10	DC-30
3	DC-30	11	DI-30
4	DN-30	12	DI-30
5	DM-30	13	DN-30
6	UF-30	14	DI-30
8	DI-30	15	DI-30
9	DI-30	23	DI-30
		26	DI-30

SIGNATURES		DATE
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DIVISION—		
BRANCH—		
BLDG.	ROOM	PHONE

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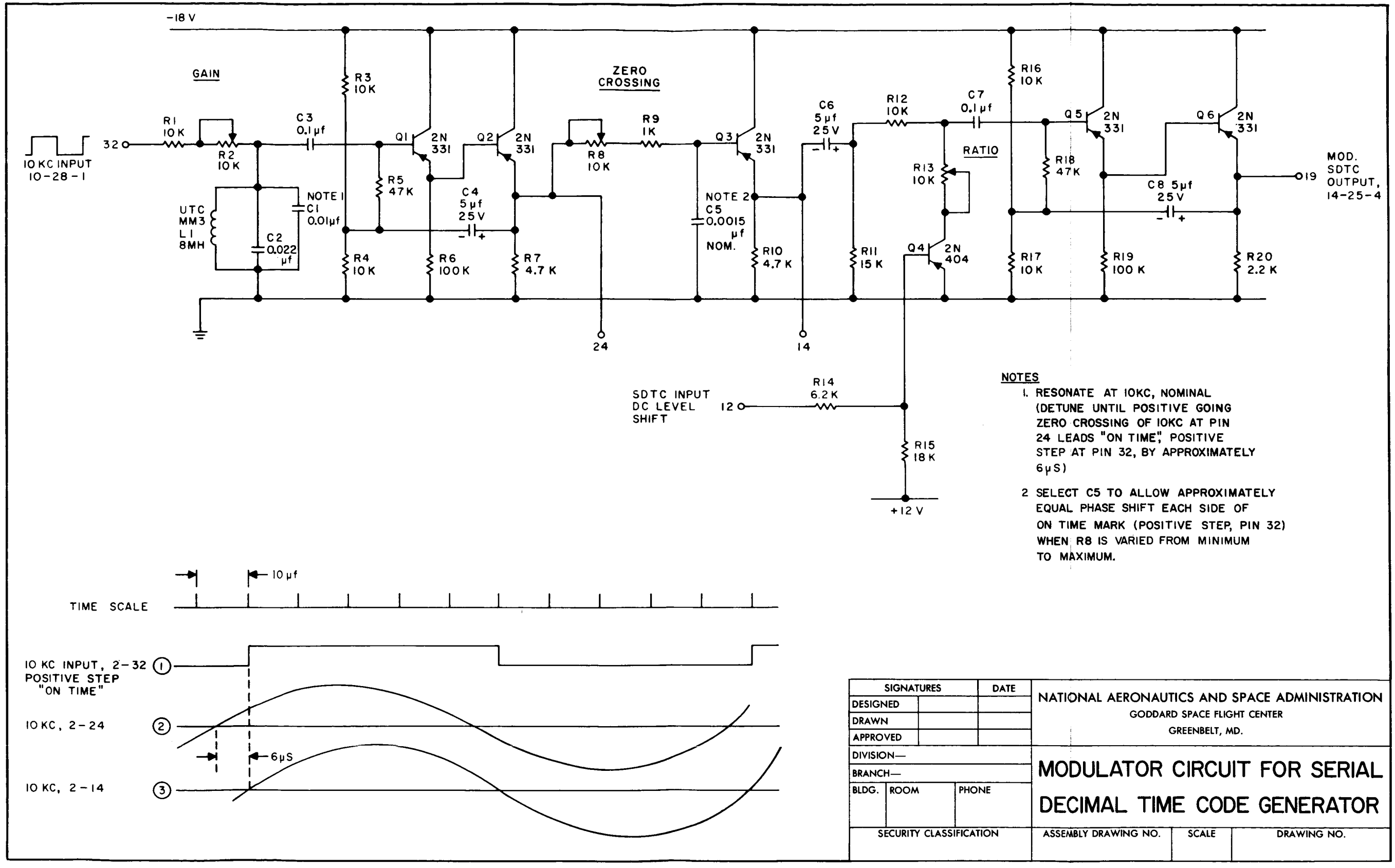
SERIAL DECIMAL TIME GENERA — TOR FUNCTIONAL BLOCK DIAGRAM SHEET 2 OF 2

SECURITY CLASSIFICATION	ASSEMBLY DRAWING NO.	SCALE	DRAWING NO.

FIGURE 6.6 SERIAL DECIMAL TIME CODE GENERATOR, FUNCTIONAL BLOCK DIAGRAM, SHEET 2 of 2



SIGNATURES		DATE
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DIVISION—		
BRANCH—		
BLDG.	ROOM	PHONE

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MODULATOR CIRCUIT FOR SERIAL DECIMAL TIME CODE GENERATOR

SECURITY CLASSIFICATION	ASSEMBLY DRAWING NO.	SCALE	DRAWING NO.

FIGURE 6-7
MODULATOR CIRCUIT FOR SERIAL DECIMAL TIME CODE GENERATOR, SCHEMATIC DIAGRAM

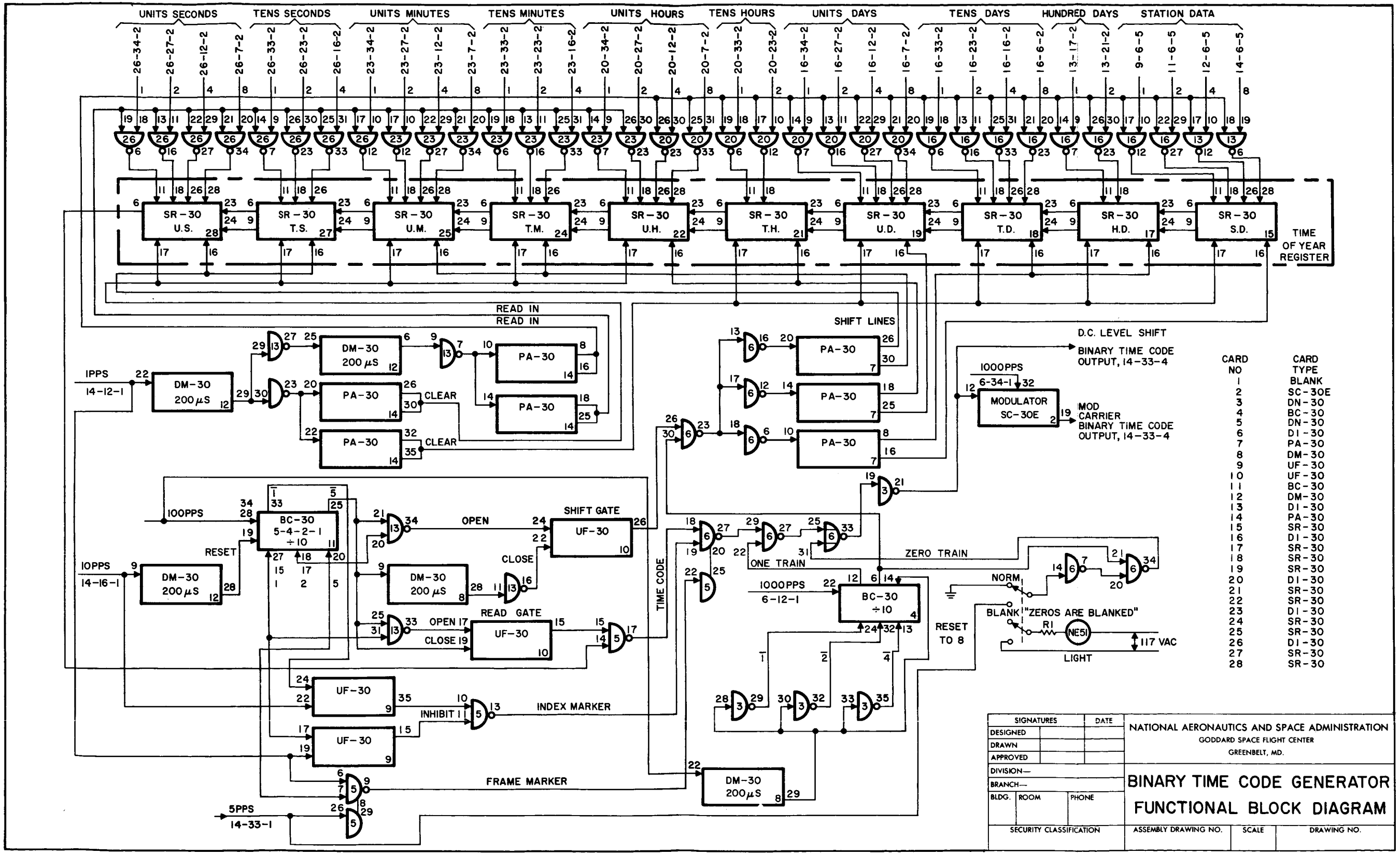


FIGURE 6-8 BINARY TIME CODE GENERATOR, FUNCTIONAL BLOCK DIAGRAM

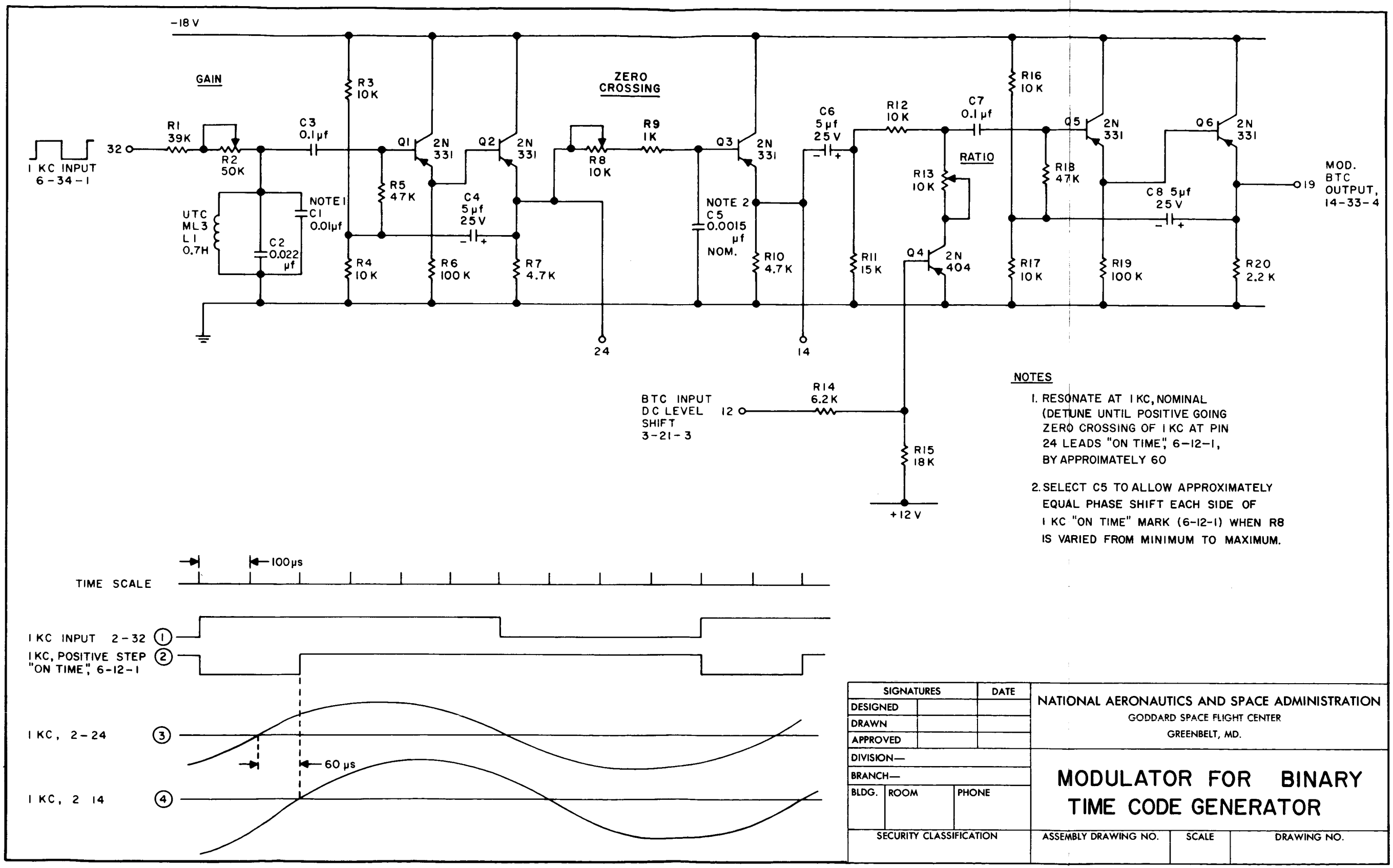
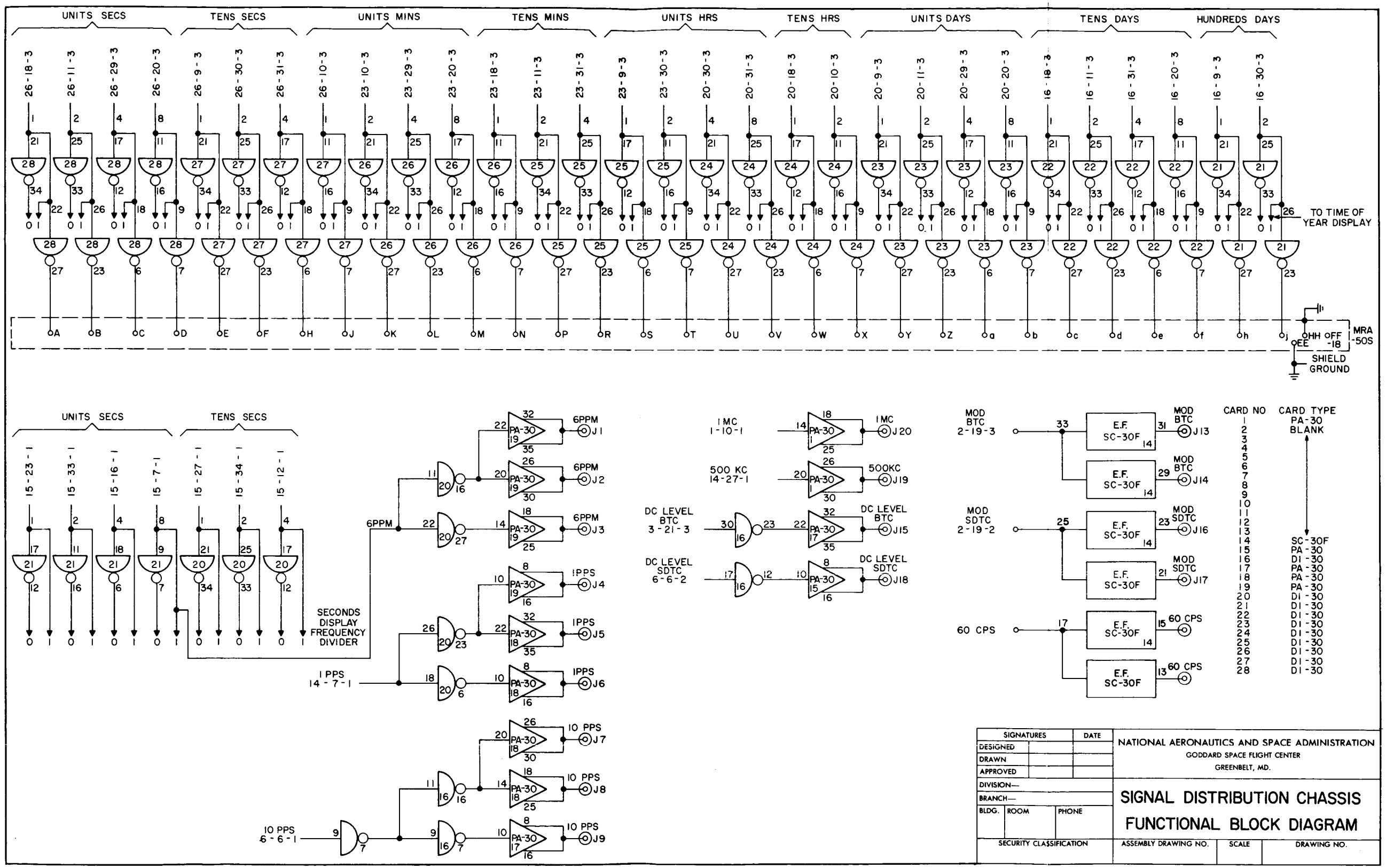


FIGURE 6-9 MODULATOR FOR BINARY TIME, CODE GENERATOR, SCHEMATIC DIAGRAM



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BLDG.	ROOM	PHONE

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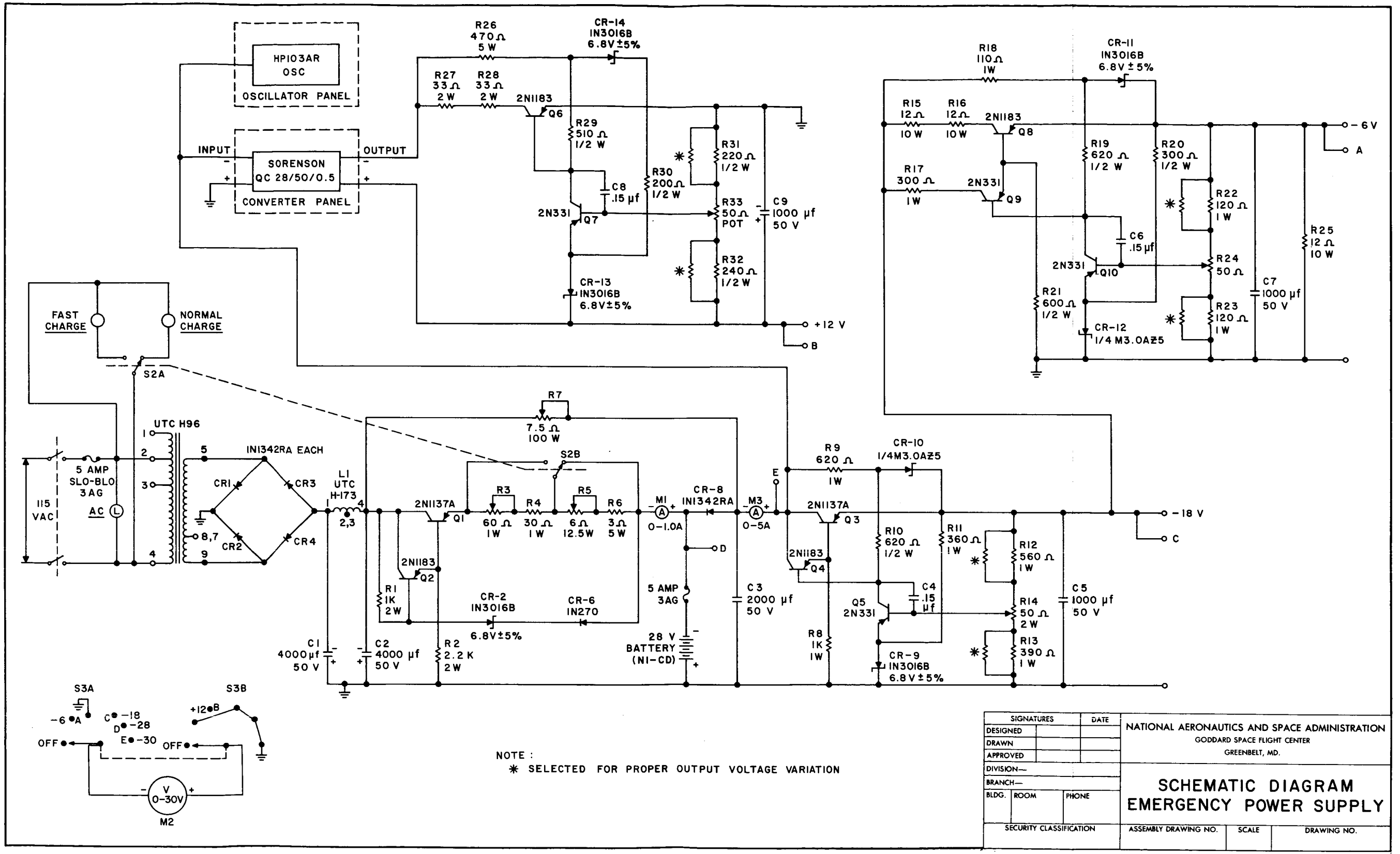
SIGNAL DISTRIBUTION CHASSIS
FUNCTIONAL BLOCK DIAGRAM

SECURITY CLASSIFICATION	ASSEMBLY DRAWING NO.	SCALE	DRAWING NO.

FIGURE 6-10 SIGNAL DISTRIBUTION CHASSIS, FUNCTIONAL BLOCK DIAGRAM



NOTE :
* SELECTED FOR PROPER OUTPUT VOLTAGE VARIATION

SIGNATURES		DATE
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DIVISION—		
BRANCH—		
BLDG.	ROOM	PHONE
SECURITY CLASSIFICATION		

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SCHEMATIC DIAGRAM
EMERGENCY POWER SUPPLY

ASSEMBLY DRAWING NO.	SCALE	DRAWING NO.

FIGURE 6-11 EMERGENCY POWER SUPPLY, SCHEMATIC DIAGRAM